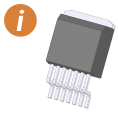
SiC JFET Surface Mount Technology Devices

AND90333/D

Introduction

Pick-and-place machines place surface mount technology (SMT) devices on a circuit board very quickly and with excellent precision. This combined with a highly repeatable solder process in a reflow oven results in low assembly cost with superior mechanical reliability. These benefits are further combined with reduced stray inductance and package resistance (better electrical and EMI performance) in SMT power devices. The use of SMT power devices is enabled in part by the low power loss of SiC devices. This application note addresses the construction, land patterns, moisture sensitivity level, and reflow solder profile for **onsemi** SMT devices.



onsemi SMT products combine the benefits of highly repeatable, low-cost manufacturing processes with excellent electrical performance.

Scope

This document provides package, land pattern, solder profile, and storage information for **onsemi** surface-mount technology (SMT) devices, including D2PAK-7L (TO-263-7L), D2PAK-3L (TO-263-3L), and TOLL (MO-229).

onsemi SMT Construction

onsemi SMT devices are constructed with a 100% matte tin plated copper lead-frame and pins, as shown in a cross-section drawing of a D2PAK-7L (TO-263-7L) below in Figure 1. The D2PAK-3L and other SMT device construction are similar. The exposed metal on the bottom side of the package, referred to as the tab, is always the electrical connection to the drain.

Most **onsemi** SMT products use silver sintered connections that maintain integrity at temperatures of several hundred degrees C, and consequently there is no concern of re-melting sintered connections during PCB assembly or rework processes. A further advantage of silver sintering versus solder is significantly reduced thermal resistance between the chip and the copper lead-frame, which results in a lower junction-case thermal resistance. The few SMT products with solder-attached chips use high-lead content, high-temperature solder that melts at 380 °C.

All **onsemi** products are RoHS compliant, even those that use solder instead of sintering. Use of lead in high melting temperature solder is allowed by the RoHS initiative.

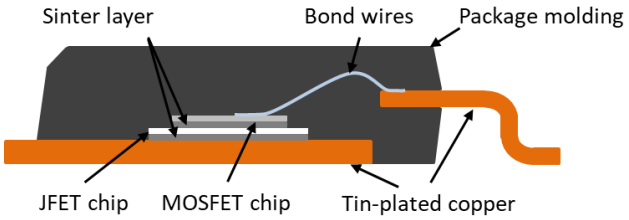


Figure 1. D2PAK-7L Cross-Section Drawing of a onsemi Cascode, Not to Scale, JFET Gate Bond Wire Omitted for Clarity

Cascode

The cascode construction is either stacked or side-by-side. The cross-section drawing of Figure 1 is that of a stacked cascode with the JFET chip silver sintered to the copper lead-frame, and the low-voltage MOSFET chip sintered directly on top of the JFET chip. The stacked cascode has the designation ‘SC’ in the part number, such as UJ4**SC**075011B7S. The letter ‘S’ at the end of the part number designates silver sinter chip attach. If this final ‘S’ is missing, then the chip attach is with high-temperature solder.

In the side-by-side construction, the low-voltage MOSFET is mounted on a ceramic substrate. The ceramic substrate is often referred to as DBC, which stands for the direct bonded copper, with the top-side copper forming a printed circuit pattern. The side-by-side configuration has only the letter ‘C’ following the Generation designator, such as UJ4**C**075033B7S. As with the stacked configuration, the letter ‘S’ at the end of the part number designates silver sinter chip attach; or high-temperature solder without it.

JFET

JFET products of course have only the JFET chip inside the package; the MOSFET chip in Figure 1 is omitted, and wires are bonded to the top of the JFET chip. As with cascode part numbers, the inclusion or omission of the letter ‘S’ at the end of the part number designates silver sinter or high-temperature solder chip attach, respectively.

PACKAGE OUTLINE DRAWINGS AND PRINTED CIRCUIT BOARD LAND PATTERNS

Following are package outline drawings (POD) and PCB land patterns for various SMT packages. Land pattern refers to the metal pads on the PCB surface where solder paste is applied. Footprint refers to the package outline as viewed from above.

D2PAK-7L

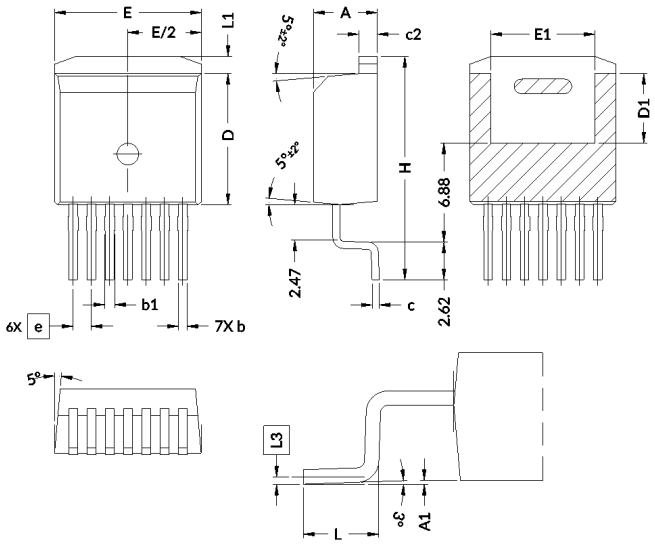


Figure 2. D2PAK-7L (TO-263-7L) Package Outline Drawing

Table 1. D2PAK-7L (TO-263-7L) PACKAGE OUTLINE DRAWING DIMENSIONS TABLE

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	8.40	8.60	8.80
A1	0.40	0.60	0.80
A2	7.90	8.00	8.10
A3	2.30	2.40	2.50
A4	3.90	4.00	4.10
A5	1.65	1.75	1.85
A6	3.40	3.50	3.60
A7		1.00 REF	
b	1.90	2.00	2.10
b1	---	---	2.80
b2		1.40 REF	
b3	---	---	2.20
b4	0.50	0.60	0.70
c	0.45	0.50	0.60
D	78.80	79.00	79.20
D1	49.50	49.70	49.90
D2	69.85	70.00	70.15
D3	34.80	35.00	35.20
D4	37.60	37.80	38.00
D5	35.66	35.86	36.06

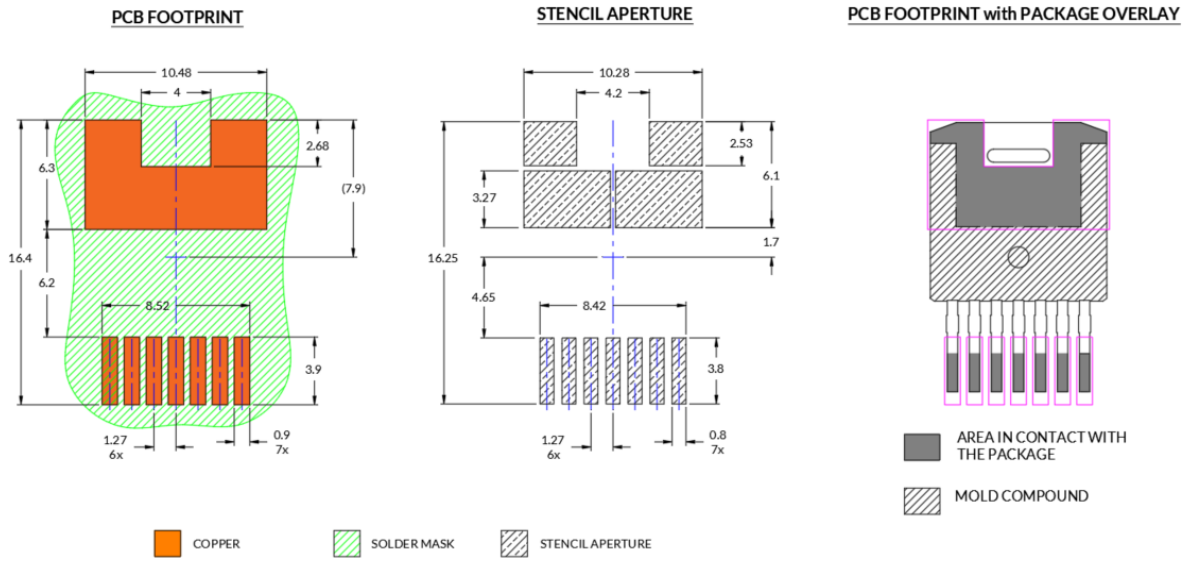


Figure 3. D2PAK-7L (a) PCB Land Pattern with Dimensions in Millimeters, (b) Footprint Overlaying Land Pattern Highlighting Area Within Land Pattern in Contact with Package Metal

D2PAK-3L

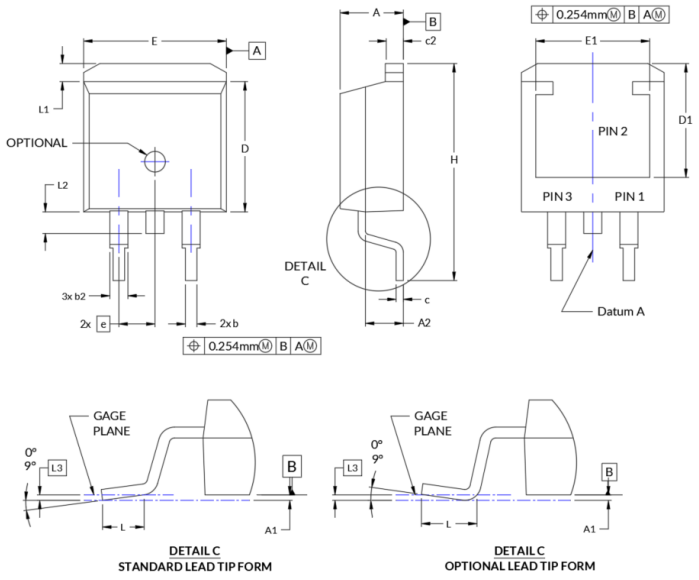


Figure 4. D2PAK-3L (TO-263-3L) Package Outline Drawing

Table 2. D2PAK-7L (TO-263-7L) PACKAGE OUTLINE DRAWING DIMENSIONS TABLE

D2PAK-3L						
Sym	mm			Inch		
	Min	Nom	Max	Min	Nom	Max
A	4.06	4.45	4.83	0.160	0.175	0.190
A1	0.00	–––	0.25	0.000	–––	0.010
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.51	0.81	0.99	0.020	0.032	0.039
b2	1.14	1.27	1.78	0.045	0.050	0.070
c	0.38	0.50	0.74	0.015	0.020	0.029
c2	1.14	1.27	1.65	0.045	0.050	0.065
D	8.38	9.14	9.65	0.330	0.360	0.380
D1	6.86	8.00	8.37	0.270	0.315	0.330
e	2.54 BSC			0.100 BSC		
E	9.65	10.03	10.67	0.380	0.395	0.420
E1	6.22	8.00	8.37	0.245	0.315	0.330
H	14.61	15.24	15.88	0.575	0.600	0.625
L	1.78	2.54	2.79	0.070	0.100	0.110
L1	1.02	1.27	1.68	0.040	0.050	0.066
L2	1.27	1.52	1.78	0.050	0.060	0.070
L3	0.25 BSC			0.010 BSC		

Notes:

1. CONTROLLING DIMENSION: **MILLIMETERS**
2. PACKAGE BODY SIDES DOES NOT INCLUDE MOLD FLASH AND GATE BURRS.
3. DIMENSION L IS MEASURED IN GAGE LINE.
4. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. PACKAGE MARKING: REFER TO DS_TO_263_3L

PIN DESIGNATIONS:

PIN 1: Source
PIN 2: Drain
PIN 3: Gate

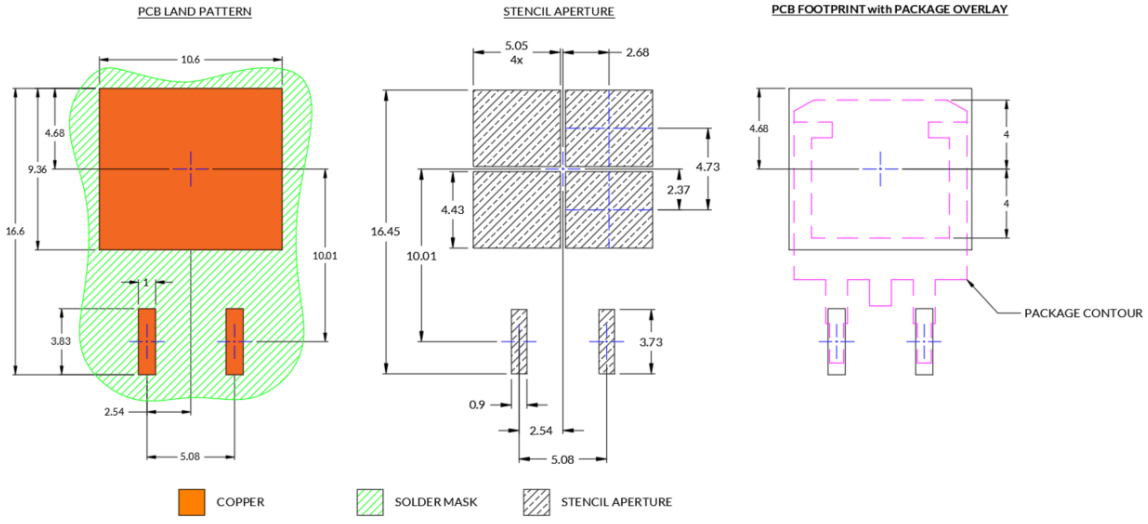
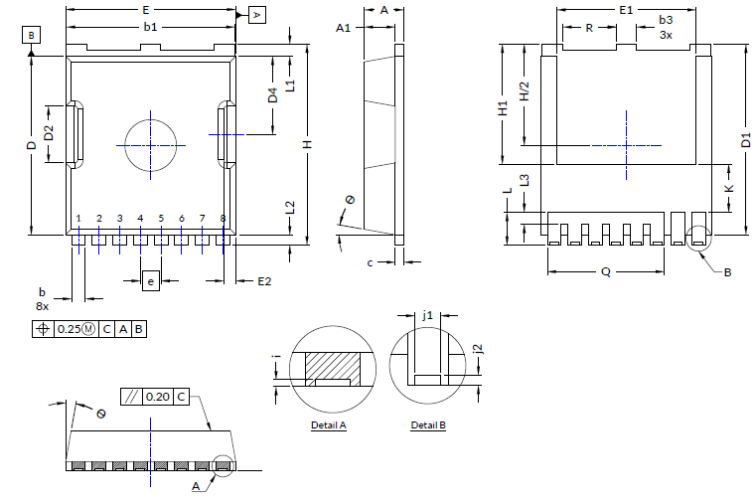


Figure 5. D2PAK-3L PCB Land Pattern with Dimensions in Millimeters

TOLL (MO-229)



Note:
1. All dimensions in millimeters
2. Dimensions does not include Burrs and Mold Flashes
3. Dimensions in compliance with JEDEC MO-299B except for backside heatsink exposed pad dimension, E1 and H1

Pin Designations:
1 : Gate
2 : Source Kelvin
3-8 : Source

Figure 6. TOLL Package Outline Drawing

Table 3. TOLL POD DIMENSIONS

TO-LL			
Symbol	Value (mm)		
	Min	Nom	Max
A	2.15	2.30	2.45
A1		1.80 REF	
b	0.70	0.80	0.90
b1	9.65	9.80	9.95
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	10.98	11.08	11.18
D2	3.15	3.30	3.45
D4	4.40	4.55	4.70
E	9.70	9.90	10.10
E1	7.95	8.10	8.25
E2	0.60	0.70	0.80
e		1.20 BSC	
H	11.48	11.68	11.88
H1	6.80	6.95	7.10
i		0.10 REF	
j1		0.46 REF	
j2		0.20 REF	
K		2.80 REF	
L	1.40	1.90	2.10
L1	0.50	0.70	0.90
L2	0.48	0.60	0.72
L3	0.30	0.70	0.80
Q		6.80 REF	
R	3.00	3.10	3.20
θ		10°	

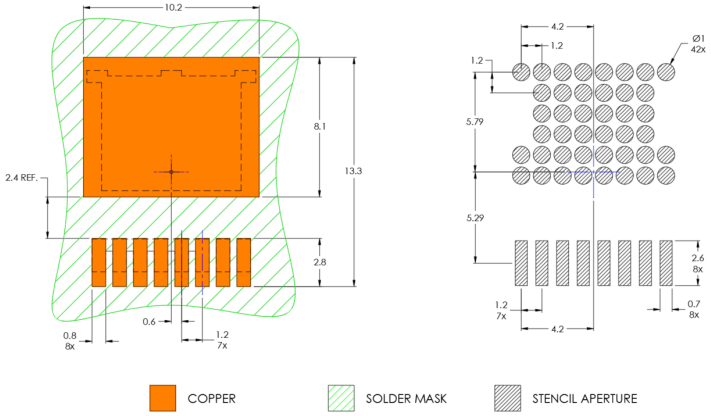


Figure 7. TOLL Land Pattern with Dimensions

Moisture Sensitivity Level (MSL)

The expansion of trapped moisture can damage SMT components during rapid temperature changes in the solder reflow process. Such damage is often not visible, but in severe cases can result bulges or external cracks. Moisture sensitivity level (MSL) is based on JEDEC standard JSTD-020 with the purpose of defining levels corresponding to proper packaging, storage, and handling to avoid damage. The MSL standard specifies the period for which a moisture sensitive device can be exposed to ambient room conditions before going through a reflow or rapid temperature-change rework process.

Table 4. MSL LEVELS AND FLOOR LIFE AT 30 °C

MSL	onsemi Parts	Floor life	Relative Humidity
1	All D2PAK-3L	Unlimited	85%
2	1	1 Year	60%
2a	0	4 Weeks	
3	1	168 Hours	
4	1	72 Hours	
5	1	48 Hours	
5a	1	24 Hours	
6	1	Time on Label (TOL) after Break	

Floor life refers to the time after product is removed from its sealed, dry, packing. Higher temperature and/or higher humidity increase moisture absorption in the SMT package and shortens the floor life. Conversely, lower temperature and/or lower humidity generally reduces moisture ingress and therefore increases the floor life.

Products that exceed their floor life can be baked dry and then run through the solder reflow process. Also, products with MSL rating of 2 or higher (more moisture sensitive) may need to be baked before certain types of rework. Refer to JEDEC standard J-STD-033 for bake conditions and time. All **onsemi** products in D2PAK-3L package are MSL1. Products in D2PAK-7L and TOLL are MSL3. Gen3 includes cascode FETs and JFETs with part numbers that begin with UJ3 or UF3.

Reflow Profile

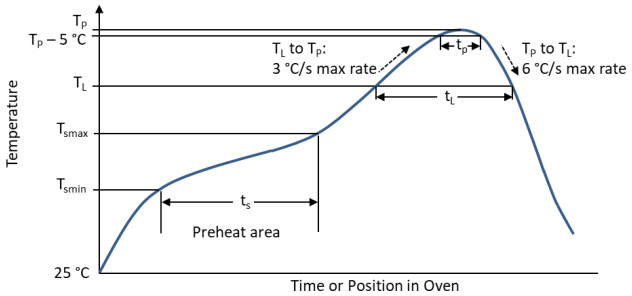


Figure 8. Reflow Profile, Referred to as Classification Profile in J-STD-020

Table 5. CLASSIFICATION PROFILES

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat Soak Temperature min (T_{smin}) Temperature min (T_{smax}) Time (ts) from T_{smin} to T_{smax}	 100 °C 150 °C 60−120 secs	 150 °C 200 °C 60−120 secs
Ramp-up Rate (T_L to T_P)	3 °C / secs maximum	
Liquidous Temperature (T_L) Time (t_L) maintained above T_L	183 °C 60−150 secs	217 °C 60−150 secs
Classification Temperature	D2PAK-3L: 220 °C D2PAK-7L: 220 °C TOLL: 235 °C	D2PAK-3L: 220 °C D2PAK-7L: 220 °C TOLL: 235 °C
Time (t_P)* within 5 °C of T_c, see Figure 8	20 secs	20 secs
Time 25 °C to peak Temperature	6 mins max.	6 mins max.

The classification temperature (TC) in is the maximum allowed peak temperature (TP), which is measured at the top of the package.

REVISION HISTORY

Revision	Description of Changes	Date
2	Replaced images with higher-resolution versions to enhance documentation quality.	11/11/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

ADDITIONAL INFORMATION

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