APPLICATION NOTE
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Over-temperature Detection Guide for the Traction Power Modules

AND90344/D

Introduction

The junction temperature of power semiconductors is one of the critical parameters limiting the output power of the traction inverter. The output power of an inverter can be controlled based on the estimated junction temperature at the given operating condition of the inverter. However, there are multiple factors that affect the junction temperature such as degraded thermal impedance of the power semiconductor, insufficient coolant flow, excessive current flowing due to partial malfunction of the inverter part, and so forth. Hence, proactive protection based on temperature monitoring is required to improve the safety of whole vehicles.

Temperature Sensors in the Power Module

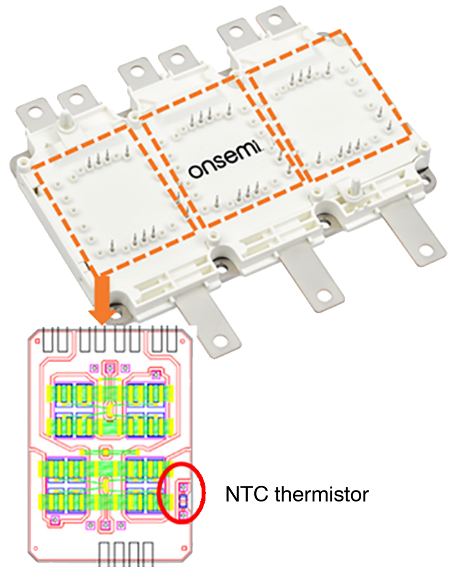
All EV traction modules from **onsemi** have a built-in temperature sensor which is either an NTC thermistor or an on-chip temperature sensing diode. If a traction power module is composed of multiple chips per functional switch, an NTC thermistor is integrated in the power module close to the power switch shown in Figure 1 (a). If the functional switch consists of a single large chip based on Silicon technology, a diode-type temperature sensor is fabricated on the chip as shown in Figure 1 (b).

Characteristics of NTC Thermistor

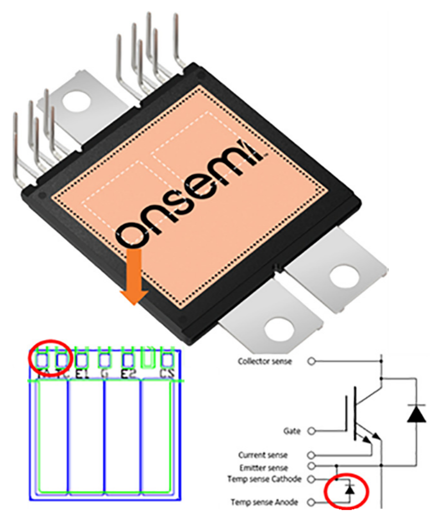
An NTC thermistor is characterized by its resistance and corresponding temperature. There are several parameters of NTC thermistors that define their characteristics such as B− and thermal dissipation constants. The B-constant characterizes the resistance with respect to temperature which is needed to design the temperature readout circuit parameters such as bias voltage and potential divider resistance. The thermal dissipation constant defines the self-heating characteristic of the thermistor required in the voltage-divider network for the thermistor. Such parameters required in the design of the sensing network are described in the datasheet for each product. A table and graph of the temperature and corresponding resistance of the NTC thermistor (shown in Figure 2) with fine resolution are also available upon request.

Characteristics of On-chip Temperature Sensor

The DSC module shown in Figure 1 (b) has a single IGBT chip per functional switch where the temperature sensing diode is integrated at the corner of the chip. The voltage drop of the temperature sensing diode is 2.5 V (typ) at T_{vj} of 25 °C and 1.7 V (typ) at 150 °C with a forward bias current of 1 mA and has a good linearity with the sensed temperature as shown in Figure 3. To ensure tight tolerance in the inverter's temperature sensing circuit, the measured voltages across temperature sensors at 25 °C and 150 °C for both high− and low−side switches can be marked as a QR code on the package upon separate request for the product.



a)



On-chip temperature sensor

b)

Figure 1. Built-in Temperature Sensors of onsemi Traction Modules (a) NTC Type in Sigle-side Direct Cooling (SSDC) Module (b) On-chip Sensor type in Dual-side Cooling (DSC) Module

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Table 1. NTC THERMISTOR CHARACTERISTICS OF SSDC MODULE FAMILY (NVH*S75L4S***, NVXR**S90M****)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{25}	Rated Resistance	T_{NTC} = 25 °C	–	5	–	kΩ
ΔR/R	Deviation of R_{100}	T_{NTC} = 25 °C, R_{25} = 5 kΩ	–5	–	5	%
P_{25}	Power Dissipation	T_{NTC} = 25 °C	–	–	20	mW
$B_{25/50}$	B-Value	R = R_{25} exp [$B_{25/50}$ (1/T–1/298)]	–	3375	–	K
$B_{25/80}$	B-Value	R = R_{25} exp [$B_{25/80}$ (1/T–1/298)]	–	3411	–	K
$B_{25/100}$	B-Value	R = R_{25} exp [$B_{25/100}$ (1/T–1/298)]	–	3433	–	K

Table 2. NTC THERMISTOR CHARACTERISTICS OF A TRANSFER-MOLDED SiC MODULE (NVVR26A120M1WS*)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{25}	Rated Resistance	T_{NTC} = 25 °C	–	10	–	kΩ
ΔR/R	Deviation of R_{100}	T_{NTC} = 100 °C, R_{100} = 877 Ω	–3	–	3	%
P_{25}	Power Dissipation	T_{NTC} = 25 °C	–	–	125	mW
$B_{25/85}$	B-Value	R = R_{25} exp [$B_{25/85}$ (1/T–1/298)]	–	3610	–	K

Ambient Temperature [°C]	Min. (kohm)	Typical Resistance [kOhm]	Max. (kOhm)
94	0.5241	0.5756	0.6307
95	0.5103	0.5608	0.6148
96	0.497	0.5465	0.5993
97	0.4841	0.5326	0.5844
98	0.4716	0.5191	0.5698
99	0.4595	0.506	0.5557
100	0.4478	0.4933	0.5421
101	0.4364	0.481	0.5288
102	0.4253	0.469	0.5159
103	0.4146	0.4574	0.5034
104	0.4042	0.4462	0.4912
105	0.3941	0.4352	0.4794
106	0.3843	0.4246	0.4679
107	0.3748	0.4143	0.4568
108	0.3656	0.4043	0.446
109	0.3566	0.3946	0.4354
110	0.348	0.3851	0.4252
111	0.3395	0.376	0.4153
112	0.3313	0.367	0.4056
113	0.3233	0.3584	0.3962
114	0.3156	0.35	0.3871
115	0.3081	0.3418	0.3782
116	0.3008	0.3338	0.3696
117	0.2937	0.3261	0.3612
118	0.2868	0.3186	0.353

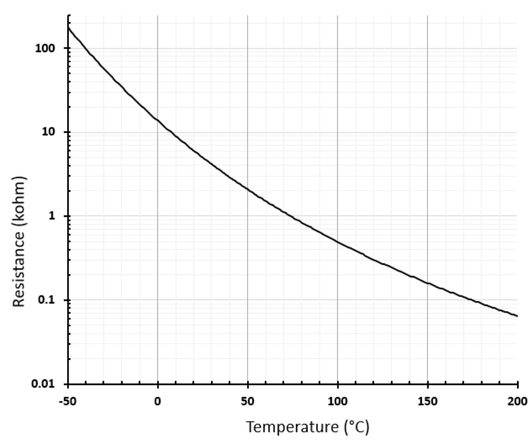


Figure 2. Table and Graph of the NTCT thermistor in SSDC Modules

SENSOR CHARACTERISTICS (T_{VJ} = 25°C, Unless Othe

	Parameters	Conditions	Typ	Unit
T_{sense}	Temperature sense	I_F = 1 mA, T_{VJ} = 25°C T_{VJ} = 150°C T_{VJ} = 175°C	2.5 1.7 1.5	V

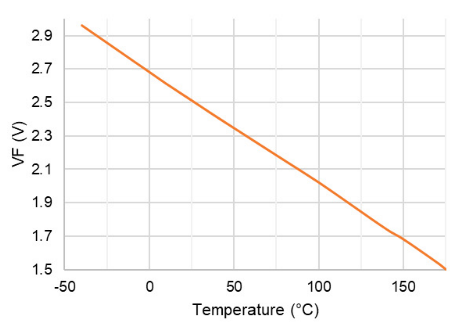


Figure 3. Temperature Sensor Characteristics of DSC Modules

Temperature Correlation Between a Switch and a Sensor

Once the characteristics of the thermal sensor are defined, temperature at the sensor can be measured using an additional bias circuit. However, the measured temperature at the sensor does not represent the junction temperature of the switch. Even if an on-chip sensor is used, there is a temperature differences between the sensor and the junction of the power semiconductor. Furthermore, because the inverter does not always operate in steady-state mode, time delay between junction temperature of the chip and the sensor temperature must be considered for safe protection against an over-temperature event. To determine the relationship between junction temperature and the sensor temperature, power loss vs. junction temperature and sensor temperature is characterized at specific cooling conditions.

Figure 4 shows the hardware setup for thermal characterization of the SiC SSDC module. DC current is applied to the D-S path of the SiC device to heat it up and the voltage drops across the SiC switch and the NTC thermistor are measured over temperature. Measured voltage responses can be correlated with temperatures by applying calibration K-factors shown in Figure 5, where K-factor is characterized under steady-state condition.

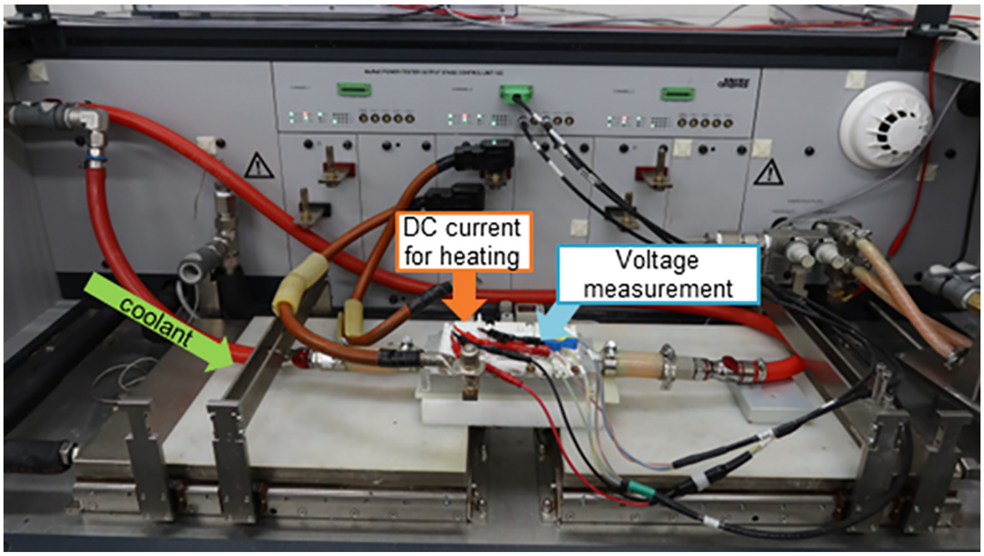


Figure 4. Thermal Characterization Hardware Setup

K-factor		
S/N	HS	LS
V phase	-2.409	-2.415
NTC	12.680	

▪ Unit: mV/°C

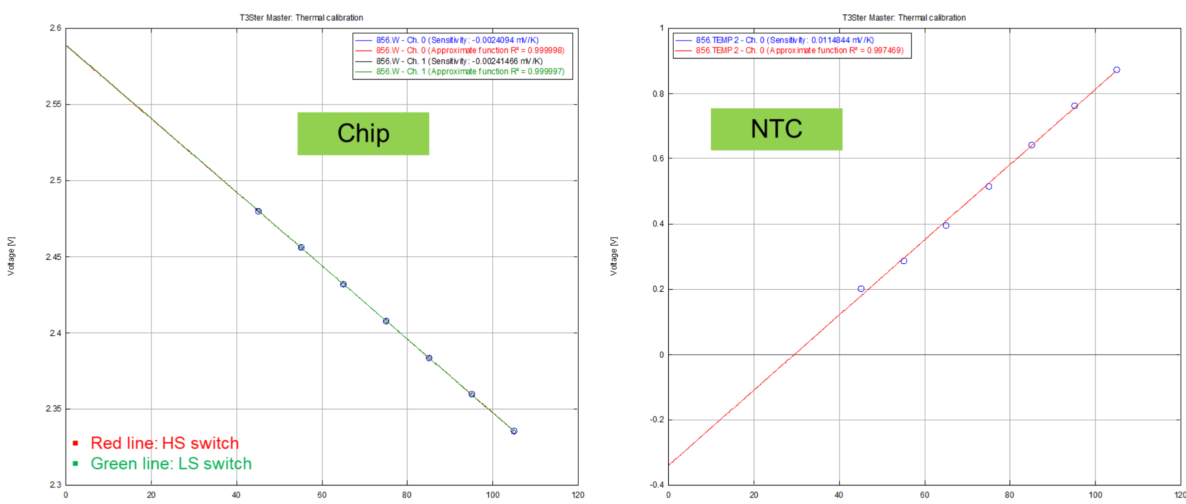


Figure 5. K-factors for SiC Chip and NTC

Once K-factors are applied to the measured voltage during cooling-down phase, the corresponding temperatures of the chip and the NTC thermistor can be represented in Figure 6. Because the thermistor is located next to the high-side switch only in the SiC SSDC module, the temperature of the thermistor is more closely correlated to the temperature of the high-side switch. By using the same temperature cool-down curve and the applied power loss on the chip, thermal impedance can be plotted as shown in Figure 7. From the thermal impedance curve, it is easy to see how much the temperature of the NTC thermistor is delayed.

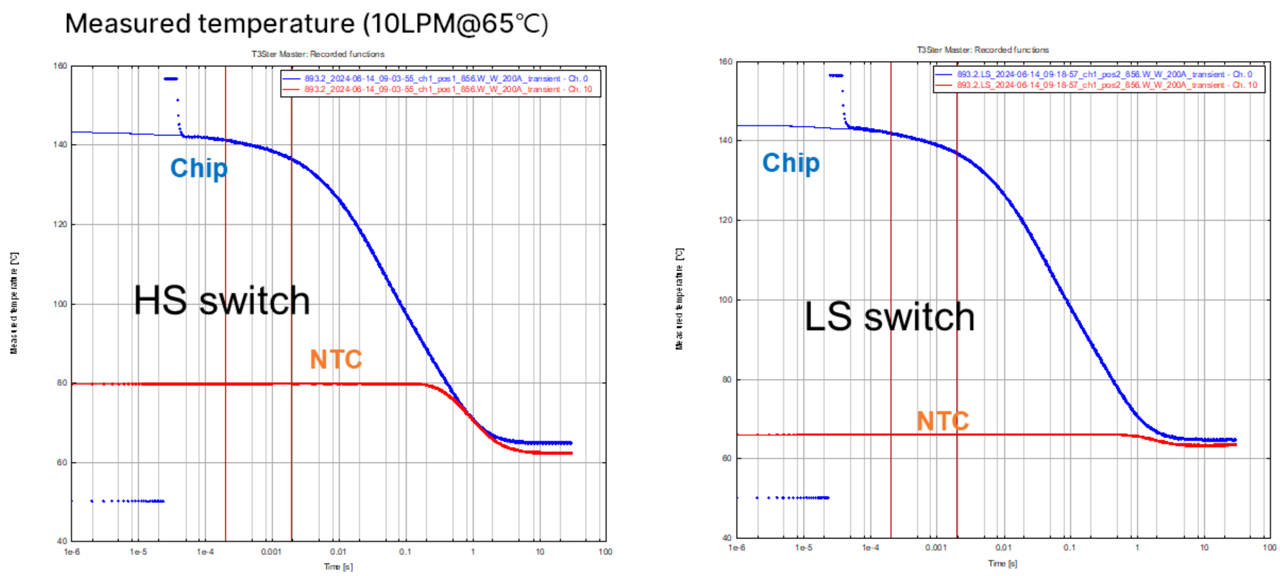


Figure 6. Temperature Measurement During Cooling Down

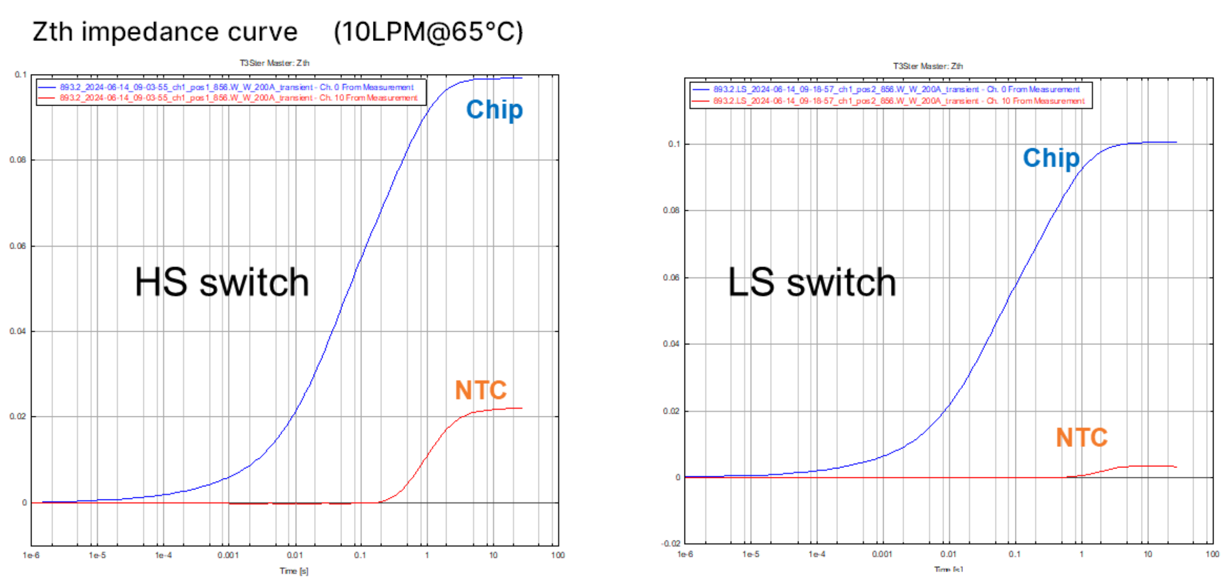


Figure 7. Thermal Impedance of the SiC Switch and the NTC Thermistor

Consideration for Temperature Sensing Delay

If the sensed temperature at the NTC thermistor represents the variation of chip temperature, thermal impedance of the thermistor can be scaled to that of the chip in terms of the steady-state value. In Figure 8, the blue and orange lines indicate the thermal impedance of the chip and the scaled thermal impedance of the thermistor. The dashed line in red shows the difference in the thermal impedances of the chip and the scaled thermal impedance of the thermistor.

Assuming that temperature is sequentially monitored at t_1 and t_2, and the corresponding change of the power loss of the switch is ΔP_{LOSS}, actual junction temperature T_j can be expressed as follows:

$$\begin{aligned} T_j(t_2) &= T_{j,\,est}(t_2) + T_{delay,\,error} \\ &= T_{j,\,est}(t_2) + \Delta P_{Loss} \cdot \Delta Z_{th,\,max} \end{aligned} \quad \text{(eq. 1)}$$

where $T_{j,\,est}(t_2)$ is the estimated junction temperature by the monitored temperature at t_2, $\Delta Z_{th,\,max}$ is the maximum discrepancy of thermal impedances of the chip and the scaled thermal impedance of the thermistor. Because $T_j(t_2)$ should be less than the target temperature $T_{j,\,target}$, (eq. 1) can be expressed in terms of ΔP_{LOSS}.

$$\Delta P_{Loss} < \frac{T_{target} - T_{j,\,est}(t_2)}{\Delta Z_{th,\,max}} \quad \text{(eq. 2)}$$

Hence, to prevent over-temperature damage, the output power must be controlled so that the power loss (ΔP_{LOSS}) of the switch meets the requirements of (eq. 2).

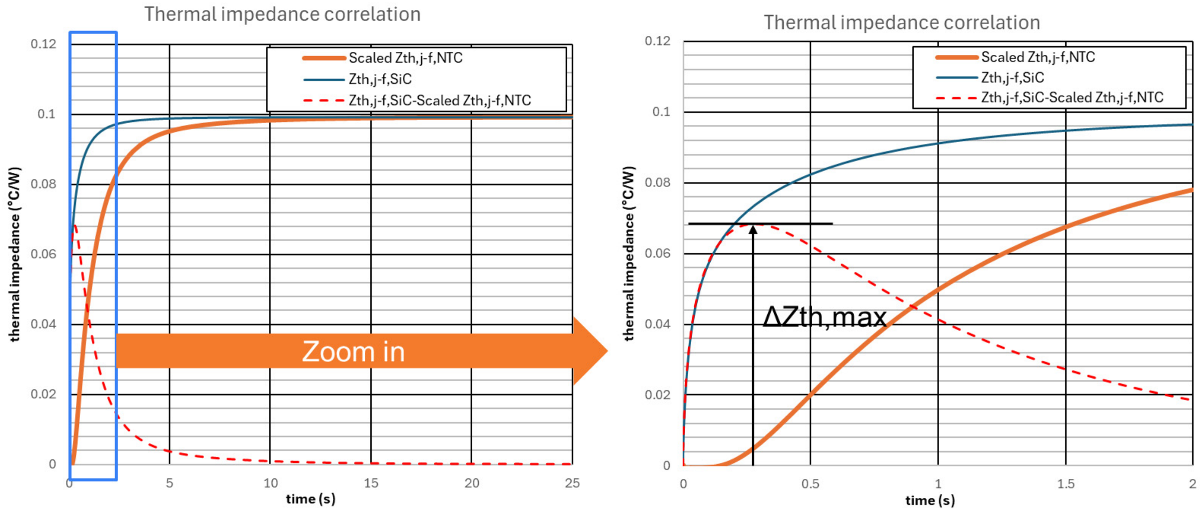
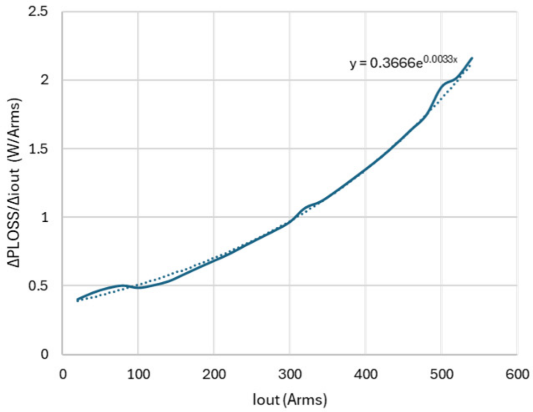


Figure 8. Thermal Impedance of the SiC Switch and the NTC Thermistor

The following case study will use the 1200 V/1.5 mΩ SiC SSDC module as an example to illustrate the power loss limitation described above. Since the magnitude of output current is the dominant factor responsible for power loss variation while the inverter is running, $\Delta P_{LOSS/switch}$ can be quantified in terms of the output current variation. Figure 9 shows the graph of $\Delta P_{LOSS/switch}$ /ΔIout when the 1200 V / 1.5 mΩ SiC SSDC module operates under the condition described in the table. When this module delivers an output current of 500 Arms, the average junction temperature of the chip is known to reach 132 °C. If T_{target} is set at 140 °C for over-temperature protection, 8 °C of temperature margin is allowed until the over-temperature protection is activated. If the output current suddenly increases at this condition and the temperature sensor is unable to respond to this transient change and capture the temperature variation due to the sensing delay, the estimated temperature of the chip will still be 132 °C. Considering $\Delta Z_{th,\,max}$ of 0.07 due to the delay of the temperature reading in Figure 8, allowable ΔP_{LOSS} from (2) is (140–132) / 0.07 = 114 W. Since ΔP_{LOSS} / ΔIout at an Iout of 500 Arms is 1.85 as per Figure 9 graph, the allowed increase in the output current is 114 / 1.85 = 61 Arms. Thus, the inverter should not increase the output current greater than 61 Arms at this condition.

Consideration for Temperature Ripple

When the temperature detection level is used for protection, the additional rise in chip temperature should be considered due to the transient ripple in the junction temperature. This temperature ripple occurs within the modulation period of the sinusoidal output current, which is too short to be detected by the thermistor. The ripple in chip temperature can be simulated using the thermal network model and the power loss during the inverter's steady state operation. Figure 10 (a) shows an example of the temperature ripple for the 1200 V / 1.5 mΩ SiC SSDC module at an output current level and frequency of 550 Arms and 40 Hz, respectively, and (b) represents the difference between peak and average junction temperature as a function of the output modulation frequency. In the example of Figure 10, if the thermistor indicates the steady-state temperature, it can be correlated to the average junction temperature of 132 °C. If the output frequency of the inverter current is 120 Hz, the peak junction temperature of the SiC device could be higher than the average temperature by ~6 °C due to the temperature ripple.



Modulation	SVPWM
VBUS	800 V
Power factor	0.9
Load frequency	120 Hz
Switching frequency	10 kHz
Modulation index	1
Coolant	50/50 Ethylene glycol, 10LPM, 65°C

Figure 9. Ration of Power Loss Variation to the Output Current Variation as a Function of the Output Current for 1200 V/1.5 mΩ SiC SSDC Module

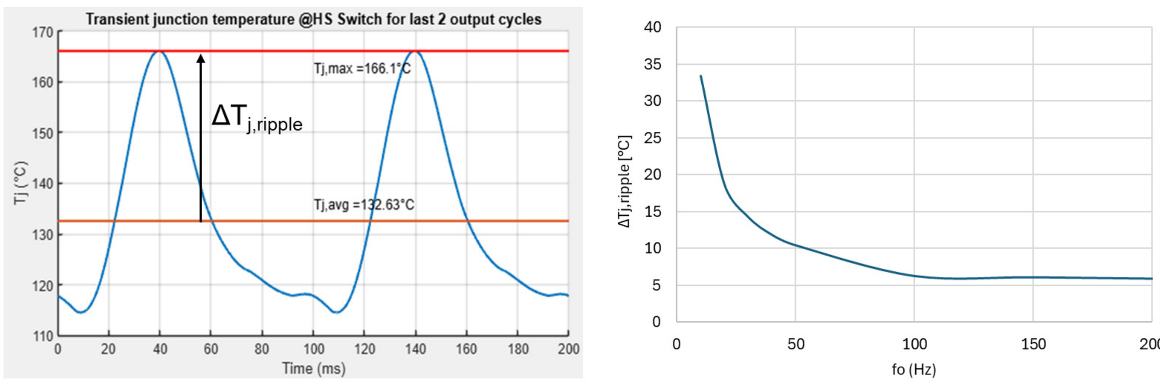


Figure 10. (a) Transient Temperature Response at the Steady State Condition of the Inverter at the Output Frequency of 40 Hz (b) Temperature Rise for the Output Frequency

Consideration for Chip-to-chip Temperature Distribution

AQG-324 guidelines for power modules recommend characterizing T_{vj} of the power semiconductor switch by measuring an equivalent voltage drop associated with temperature. However, if a functional switch comprises of multiple SiC chips in parallel, T_{vj} as defined in AQG-324 only shows the average temperature across the chips, as temperature is not uniformly distributed over the switch area. Figure 11 shows the layout of the SSDC SiC module, an FEM simulation result for the thermal distribution, an experimental setup, and the corresponding result. Because thermal impedance is characterized by means of the T_{vj}, that is, average temperature across the chips, a practical thermal impedance value can be defined using the $T_{j,max}$ across the chips. $T_{j,\,max}$ can either be estimated by performing an FEM simulation or measured using a thermal camera if the chip surface is visible.

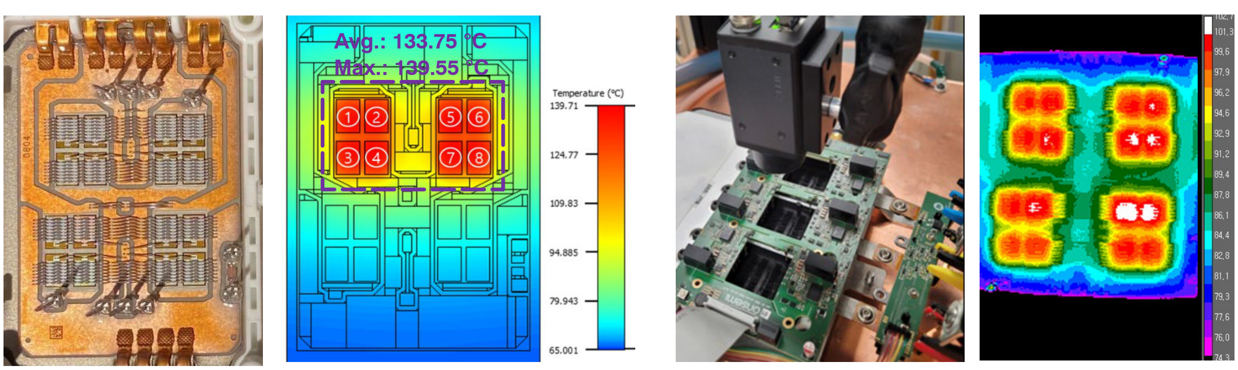
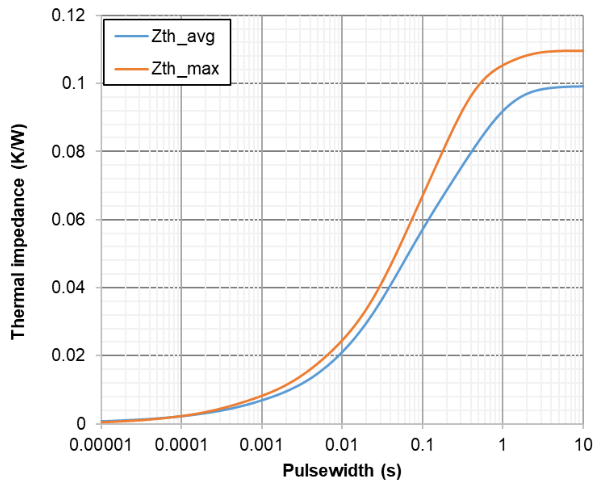
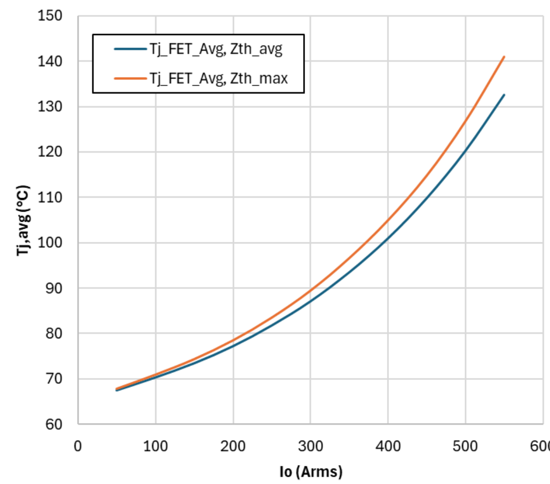


Figure 11. Temperature Distributions of the SiC SSDC Module – Simulation and Measurement Results

By applying the average and the maximum temperature over the chips, transient thermal impedance can be characterized as shown in Figure 12 (a). By applying thermal impedances in the inverter simulation, time-averaged temperatures can be estimated as shown in Figure 12 (b), where the same module and inverter operating conditions are applied as in the previous section. At an output current of 550 Arms, the difference between both temperatures is ~8.4 °C, which indicates the temperature at the hottest spot across the chips is higher than the average temperature by ~8.4 °C.



(a)



(b)

Figure 12. (a) Zth,avg, from the Average Junction Temperature, and Zth,max, from the Maximum Temperature (b) The Average Temperature of the SiC Switch from the Inverter Simulation with Zth,avg and Zth,max

Conclusion

When a built-in temperature sensor monitors the chip temperature of a power module, the monitored temperature may be lower than the highest temperature on the chip. This discrepancy can occur due to the sensor's time delay, the dimensional distribution of temperature across the entire area of chips connected in parallel, and temperature variations resulting from the output modulation frequency. The discrepancy in monitored temperature resulting from measurement delay can be estimated using the scaled thermal impedance of the temperature sensor, which can be a reference value to limit the increase in the output current. The temperature difference due to non-uniform thermal distribution across the entire area of multiple chips can be estimated by applying the thermal impedance for the hottest spot, which can be simulated using the FEM method. Additionally, a temperature gap can occur due to fluctuations in the output modulation frequency, which can be estimated using inverter simulation for steady-state operation. By estimating all the discrepancies in the monitored temperature, the detection level for over-temperature can be set at a more practical level.

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