Application Report
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Comparing Bus Solutions

F. Alicke; F. Bartholdy; S. Blozis;
F. Dehmelt; P. Forstner; N. Holland;
J. Huchzermeier

MSLP Europe

ABSTRACT

This report is intended to be a reference tool for finding the most appropriate bus interface solution for today's advanced system architecture.

This paper focuses on bus interface solutions for different backplane applications. It gives an overview of the different bus solutions available from Texas Instruments (TI™).

Today, advanced bus systems designers have a problem: many different solutions can be used to solve the same problem. The task for the designers is to figure out the optimum solution for their special application.

In order to ease this choice, this application report has been created. The different key parameters are composed in a way that developers may easily find the optimum bus solution for their systems.

The report is split into product family sections to allow easy distinction between various solutions. Each family-section of this report covers details on the electrical parameters and appropriate protocols, as well as application and feature-benefit information on the chosen product family.

All sections are set up in the same order, such that fast comparison and selection of the most appropriate solution is possible.

Keywords: ABT, AHC, BTL, CompactPCI™, FlatLink™, Gigabit, GTL, IEEE1284, IEEE1394, USB, LVDM, LVDS, LVT, PCI, TIA/EIA-232-F (RS–232), TIA/EIA-422-B (RS-422), TIA/EIA-485-A (RS-485), and TIA/EIA-644, SCSI, SERDES, SSTL, GTLP, GTL+, ALVT, FB+, ABTE.

Contents

List of Figures

List of Tables

Overview

In today's information-hungry society, transmitting data over several inches between computer memory and display screen is just as critical as sending it halfway around the globe. Over the past three decades, Texas Instruments has combined its expertise in high-speed digital and analog technologies. TI is constantly pushing the capabilities and extending the performance parameters of practically every data transmission standard, including TIA/EIA-232, TIA/EIA-423, TIA/EIA-422, TIA/EIA-485, Fibre Channel, electrical characteristics of low voltage differential signaling (LVDS), IEEE 1394 (FireWire™/i.LINK), universal serial bus (USB), GeoPort™ and Infrared Data Association (IrDA).

This application report provides the reader with an overview of the different bus systems available today and should give enough insight into which standard or which bus configuration would suit the customer's needs. Before we discuss each standard, its technical features, and the products that TI offers, it is important to understand the fundamentals behind the different bus configurations available.

Typically, data transmission, as the name suggests, is a means of moving data from one location to another. In general, there are two main parameters that define how the information is transferred. These parameters are the distance, the space between the sending and the receiving systems and speed, and the rate at which data has to be passed to the receiving device. Different transmission standards, such as TIA/EIA-232, IEEE 1394 and LVDS, provide solutions for various needs in terms of speed and line length as defined by Figure 1.

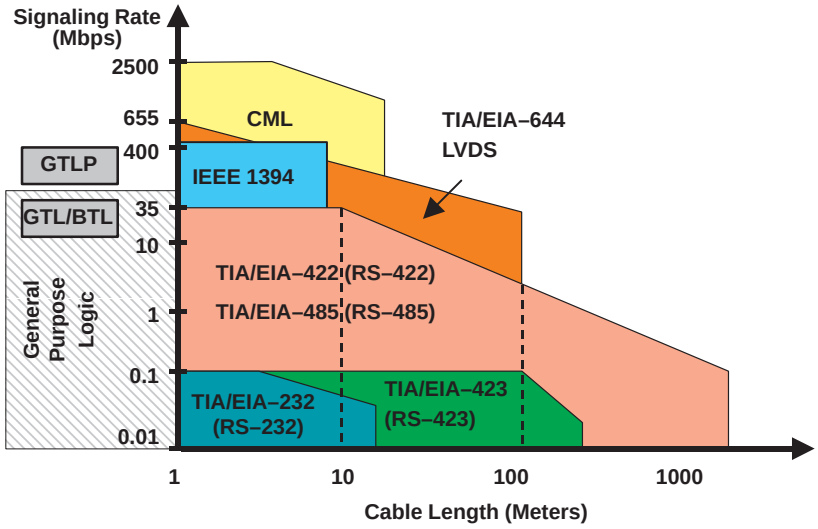


Figure 1. Signaling Rate Versus Cable Length

It can be seen from Figure 1, that, as the cable length increases, the speed at which the information is transmitted must be lowered in order to keep the bit error rate down. Therefore, it is very important to choose the correct standard covering the required communication distance and the needed data rate. Once the choice of standard has been made, the selection of the device required for the specific application can begin. This is not an easy task.

FireWire and GeoPort are trademarks of Apple Computer, Inc.

The matrix on the following page has been generated to give a more accurate overview of the different kind of transmission types, the modes, standards, distances, data rates, its benefits, and which TI family would suit which purpose. For every family, Texas Instruments has created a section within this application report describing the characteristics of the standard, whether or not there is a software overhead. There is, of course, also a family-dedicated web page, which contains further information on product datasheets, additional application reports, and the possibility of sampling devices via the Internet. The family link is also listed in the matrix.

Table 1. Bus Interface Selection Guide

TYPE	TRANSMISSION MODE	DATA RATE PER LINE	DATA RATE PER DEVICE	DISTANCE	STANDARD	PRODUCT FAMILY	WEB PAGE http://www/ti/com/sc
Serial	Multipoint	25/50 Mbps		1.5 m	IEEE1394-1995	IEEE1394 Backplane	/1394
		100 – 400 Mbps		4.5 m	IEEE1394-1995/ P1394.a	IEEE1394 Cable	
		12 Mbps		5 m	USB 1.1	USB	/usb
		35 Mbps		10 m (1200 m)	TIA/EIA 485 (ISO8482)	TIAEIA 485	/docs/products/msp/ datatran/index.htm
		200 Mbps		0.5 m	In definition	LVDM	
	Multidrop	10 MBps		10 m (1200 m)	TIA/EIA 422 (ITU-T V.11)	TIA/EIA-422	/docs/products/msp/ datatran/index.htm
		200/100 Mbps	4 ch: 800/ 400 Mbps	0.5 m/10 m	TIA/EIA-644/ TIA/EIA-644 (LVDS) /in definition	LVDS/LVDM	
	Point-to-point	512 Kbps		20 m	TIA/EIA-232 (ITU-T V.28)	TIA/EIA-232	/docs/products/msp/ datatran/index.htm
Serial	Point-to-point	400/200 Mbps	4 ch: 1600/ 800 Mbps	1 m/ 10 m	TIA/EIA-644/ TIA/EIA-644 (LVDS)	LVDS	/docs/products/msp/ datatran/index.htm
Parallel-to-serial Serial-to-parallel	Point-to-point	455 Mbps	4 ch: 1.83 Gbps	< 10 m	TIA/EIA-644/ TIA/EIA-644 (LVDS)	LVDS SerDes/FlatLink	/serdes
		1.25 Gbps	1.25 Gpbs full duplex	< 10 m	IEEE P802.3z	Gigabit Ethernet	
		2.5 Gbps	2.5 Gbps full duplex	< 10 m	IEEE P802.3z extended 2 Gbps	Serial Gigabit CMOS	
Parallel	Multipoint	35 Mbps		10 m (1200 m)	TIA/EIA-485 (ISO8482)	TIA/EIA-485	/docs/products/msp/ datatran/index.htm
		40/20 MHz	9 ch: 360/ 180 Mbps	12 m/25 m	SCSI (ISO/IEC9316)	SCSI	
		40 Mbps	9 ch: 360 Mbps	12 m	LVD-SCSI (1142-D SPI-2)	LVD-SCSI	
		200 s/100 Mbps		0.5 m/10 m	In definition	LVDM	
		33/66 MHz		0.2 m	PCI Compact	PCI	/pci
		33/66 MHz		0.2 m	PCI	PCI	
		4 MHz CLK	16 ch: 64 Mbps	10 m	IEEE Std 1284-1994	AC1284, LVC161284, LV161284	/logic
		20 MHz CLK	32 ch: 640 Mbps	0.5 m	CMOS, JESD20, TTL IEEE 1014-1987	AC, AHC, ABT	/logic
		33 MHz CLK	20 ch: 660 Mbps	0.5 m	LVTTL as stated in JEDS8-A, June 1994, IEEE 1014-1987	LVTH, ALVT	/alvt /lvt
		40 MHz CLK	16 ch: 640 Mbps	0.5 m	VME64 Standard ANSI/VITA1-1991	ABTE	/logic
		60 MHz CLK	16 ch: 960 Mbps	0.5 m	IEEE Std 1194.1-1991	BTL/FB+	
		60 MHz CLK	18 ch: 1.08 Gbps	0.5 m	JESD8-3	GTL/GTL+	/gtl
		100 MHz CLK	18 ch: 1.8 Gbps	0.5 m	JESD8-3	GTLP	/gflp
		200 MHz CLK	18 ch: 3.6 Gbps	0.1 m	EIA/JESD8-8, EIA/JESD8-9	SSTL	/logic

Single-Ended Versus Differential Data Transmission

Moving on to the electrical standards, they are currently two main configurations, single-ended (or unbalanced) and differential (or balanced data transmission). The difference between single-ended and differential transmissions is essentially described below.

Single-Ended Transmission

Single-ended transmission is performed on one signal line, and the logical state is interpreted with respect to ground. For simple, low-speed interfaces, a common ground return path is sufficient; for more advanced interfaces featuring higher speeds and heavier loads, a single return path for each signaling line (twisted pair cable) is recommended. Figure 2 shows the electrical schematic diagram of a single-ended transmission system.

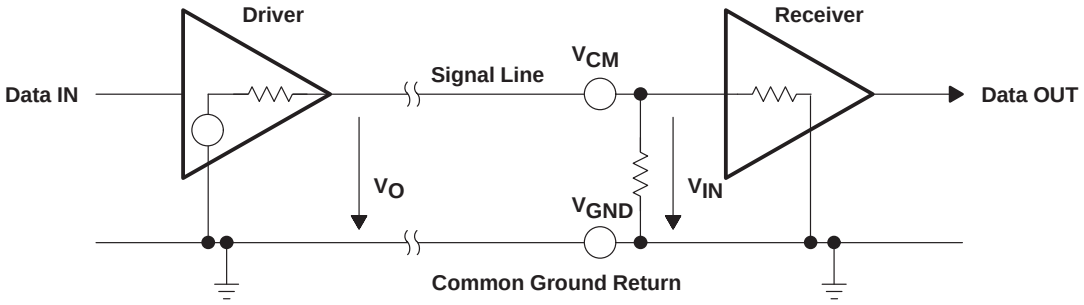


Figure 2. Single-Ended Transmission With Parallel Termination at Line End

Advantages of Single-Ended Transmission

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires only one line per signal. It is therefore ideal for cabling, and connector costs are more important than the data transfer rate, e.g. PC, parallel printer port or serial communication with many handshaking lines, e.g. EIA-232. Cabling costs can be kept to a minimum with short distance communication, depending on data throughput, requiring no more than a low cost ribbon cable. For longer distances and/or noisy environments, shielding and additional ground lines are essential. Twisted pair cables are recommended for line lengths of more than 1 meter.

Disadvantages of Single-Ended Transmission

The main disadvantage of the single-ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation. This may lead to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the signal, sufficient to drive the input across the thresholds of the receiver, thus increasing its susceptibility to electromagnetic fields.

Crosstalk is also a major concern especially at high frequencies. Crosstalk is generated from both capacitive and inductive coupling between signal lines. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high, the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow. Single-ended transmission is much more susceptible to external noise and the radiation of EMI is increased compared to differential systems.

These problems will normally limit the distance and speed of reliable operation for a single-ended link.

Differential Transmission

For balanced or differential transmission, a pair of signal lines is necessary for each channel. On one line, a true signal is transmitted, while on the second one, the inverted signal is transmitted. The receiver detects voltage difference between the inputs and switches the output depending on which input line is more positive. As shown in Figure 3, there is additionally a ground return path.

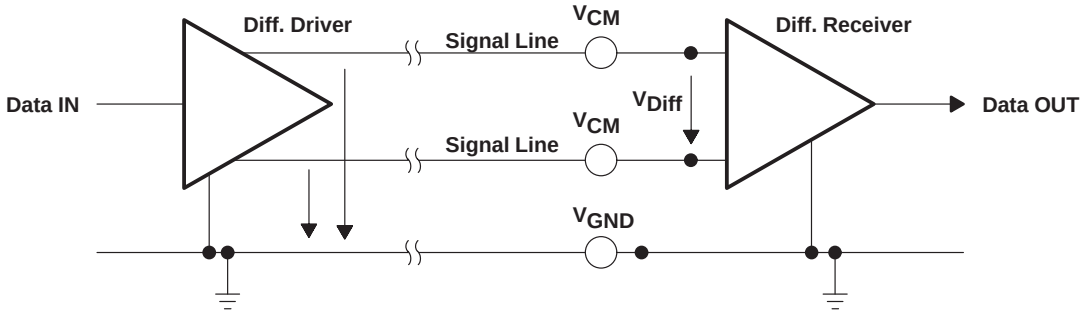


Figure 3. Differential Transmission

Balanced interface circuits consist of a generator with differential outputs and a receiver with differential inputs. Better noise performance stems from the fact that noise is coupled into both wires of the signal pair in much the same way and is common to both signals. Due to the common mode rejection capability of a differential amplifier, this noise will be rejected. Additionally, since the signal line emits the opposite signal like the adjacent signal return line, the emissions cancel each other. This is true in any case for crosstalk from and to neighboring signal lines. It is also true for noise from other sources as long as the common mode voltage does not go beyond the common mode range of the receiver. Since ground noise is also common to both signals, the receiver rejects this noise as well. The twisted pair cable used in these interfaces in combination with a correct line termination—to avoid line reflections—allows very high data rates of more than 10 Mbps and a cable length of up to 1200 m. Most recent standards allow up to 2.5 Gbps.

Advantages of Differential Transmission

Differential data transmission schemes are less susceptible to common-mode noise than single-ended schemes. Because this kind of transmission uses two wires with opposite current and voltage swings compared to only one wire for single-ended, any external noise is coupled onto the two wires as a common mode voltage and is rejected by the receivers. This two-wire approach with opposite current and voltage swings also radiates less electro-magnetic interference (EMI) noise than single-ended signals due to the canceling of magnetic fields.

Disadvantages of Differential Transmission

Great efforts have been made to further reduce the costs of these complex devices by developing them in a CMOS process, or to improve performance by using LinBiCMOS processes as for example for LVDS (further information on process technologies can be found at http:\\www.ti.com). Furthermore, the high data-rates that are possible with differential transmission require a very well-defined line impedance and correct line termination to avoid line reflections. For this method of transmission twisted pair cables instead of less expensive multi-conductor cables are recommended.

Standard Switching Levels

All standards are defined through input and output switching levels. Some of these levels are defined by the Joint Electron Device Engineering Council, otherwise known as JEDEC, and others are specified in the corresponding standard. Figure 4 shows the single-ended switching levels.

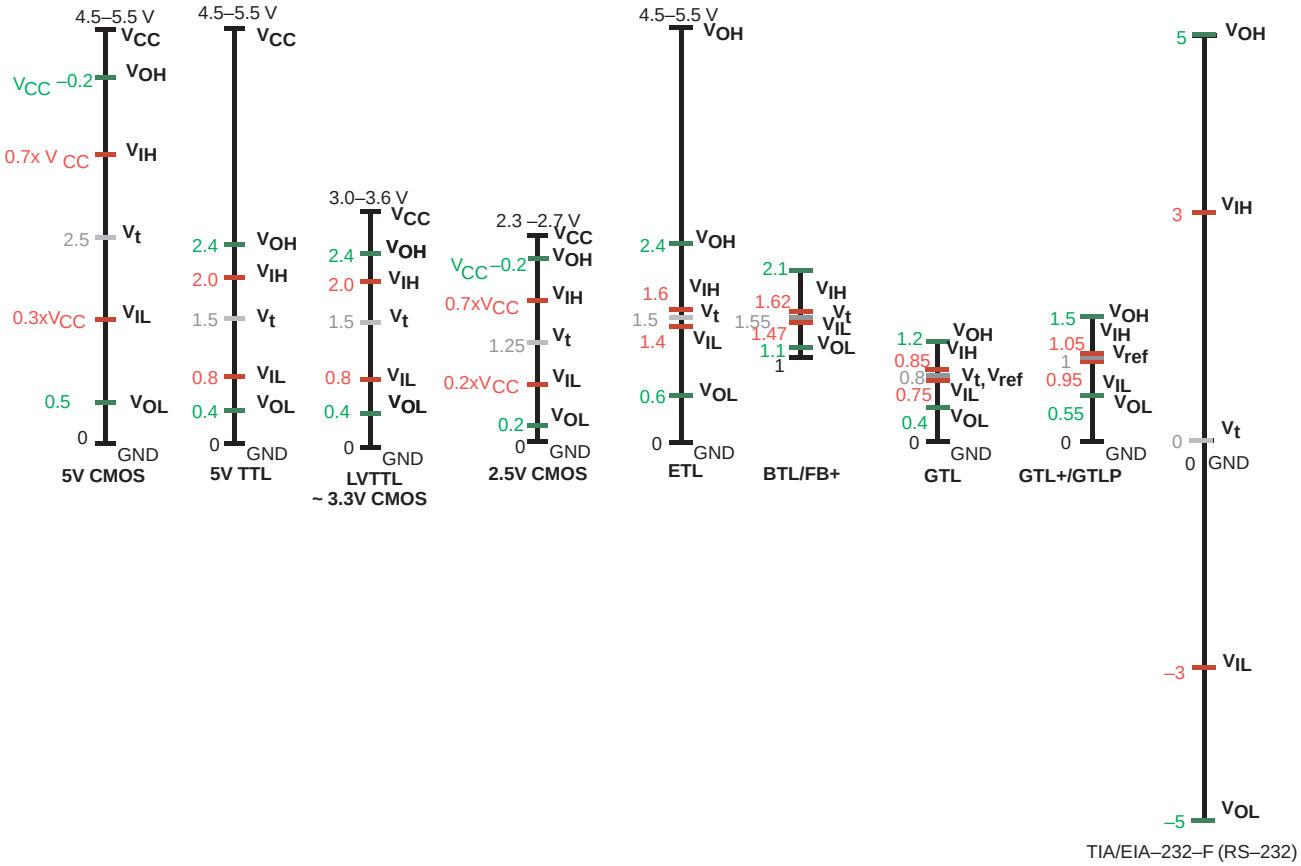


Figure 4. Switching Levels of Single-Ended Transmission Standards

The other set of switching levels applies to the differential or balanced technologies and are shown in Figure 5.

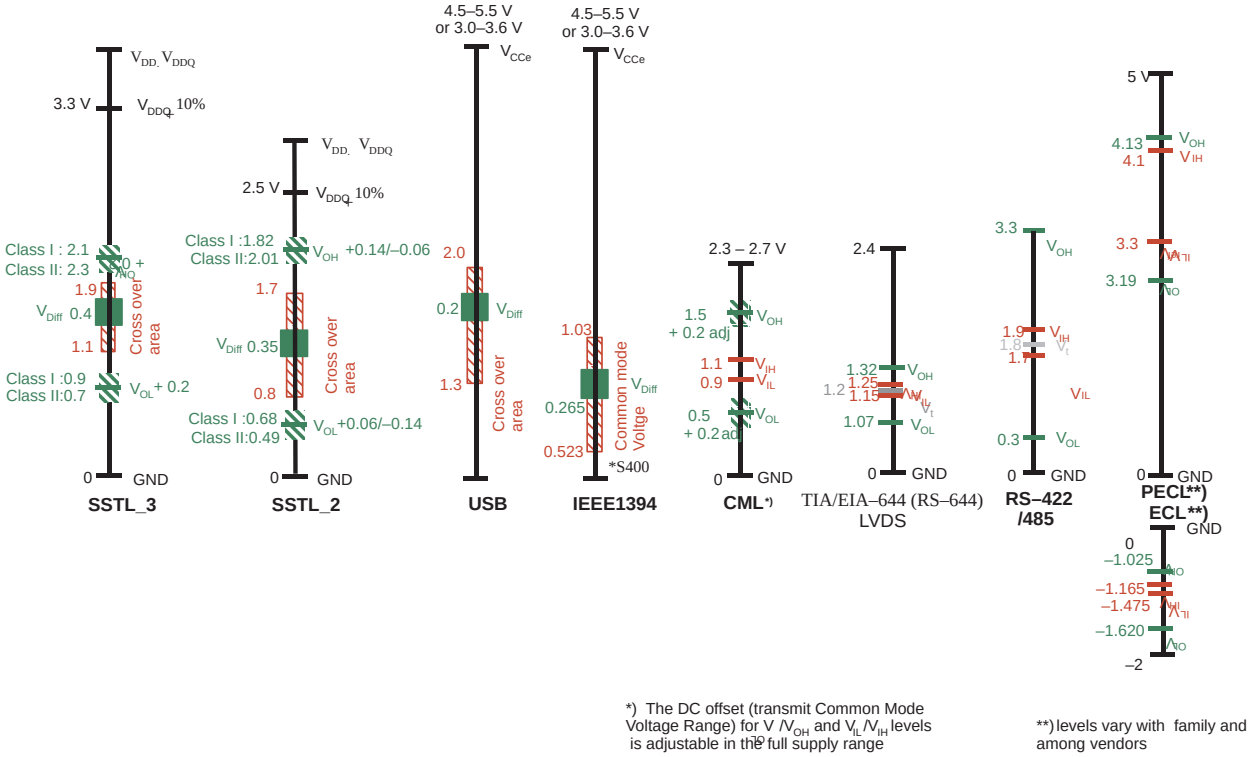


Figure 5. Switching Levels of Differential Transmission Standards

Interconnectivity

Within a data transmission system, there are numerous ways of connecting the transmitters, receivers, boards, and backplanes. Figure 6 shows how in a typical backplane rack, the cards can be linked up. The backplane itself consists of a parallel bus type configuration with each card slotted onto that bus via a connector. In some situations, it is necessary to connect either individual cards together, or a backplane to a card, etc. It would be very inconvenient to connect these devices together via a parallel cable. Serial techniques supporting a very high data rate cope with this kind of need.

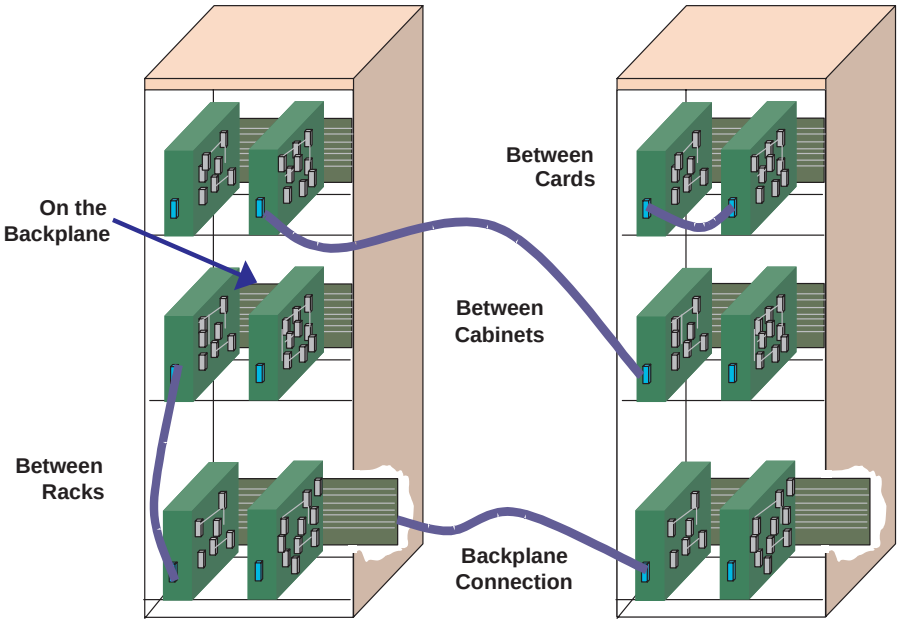


Figure 6. Different Interconnection Scenarios

LVDS is one of the latest standards that has been developed for high-speed point-to-point serial transmission. What are the benefits of serial transmission compared to parallel transmission? The next section explains the principle behind the two different techniques and outlines the benefits and shortcomings of both of them.

Parallel Versus Serial Transmission

In order to understand the principle of parallel and serial transmission, Figure 7 explains in simple terms the difference between the two. In a purely parallel situation, such as a typical telecom backplane, the driver attached to the bus places n-bits of data in parallel onto the bus and all the information is sent at the same time along the backplane.

In the case of serial transmission, the data must first be converted to a serial stream. This is called the serialization. The serial data is then transmitted at high speed along the line to the receiver, which must then deserialize the information back into the original parallel data. In order for the serial technique to achieve the same data rates as the parallel one, the data must be sent along the line at a much higher speed than on the parallel bus. However, both methods have their advantages and disadvantages.

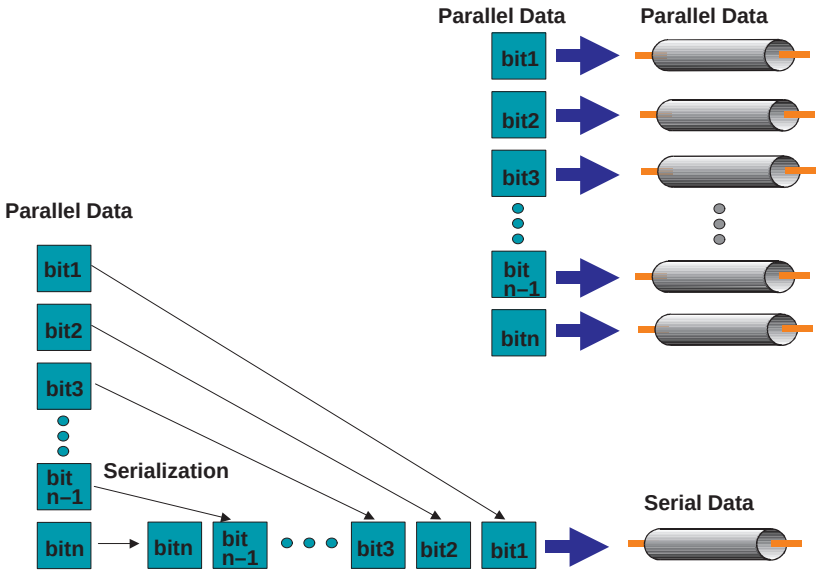


Figure 7. Principle of Parallel and Serial Transmission

Advantages of Parallel Transmission

- Parallel busses do not necessarily have the time delay required by serial busses to accumulate and decode a whole bock of data. Single lines can be configured for controlling purposes, enabling a faster reaction time.
- Many industrial and telecom applications already use parallel backplanes. This means that many designers and engineers are familiar with these kinds of systems and have the knowledge and the experience to quickly implement such systems.

Advantages of Serial Transmission

- Fewer or no problems with line-to-line signal skew
- Serial data offers a more flexible approach to data rates allowing longer cable lengths and cheaper cable costs.
- Reduction in the number of signal lines and GND lines required to transmit the data from one point to another
- Major savings on board space

Various Widely Used Data Transmission Topologies

There are currently many different methods or topologies to transmit data across wires. In this report, three main ones will be highlighted and briefly explained.

We have split this page into two columns, the left column shows the single-ended solution and the differential solution is shown in the right column. To start, we will take point-to-point connection, the principle setup for the single-ended and differential solution is shown in Figure 8.

Point-to-Point: This configuration is implemented with one transmitter and one receiver per line.

Figure 8. Point-to-Point Connection

Multi-Drop: This configuration is implemented with one transmitter and many receivers per line.

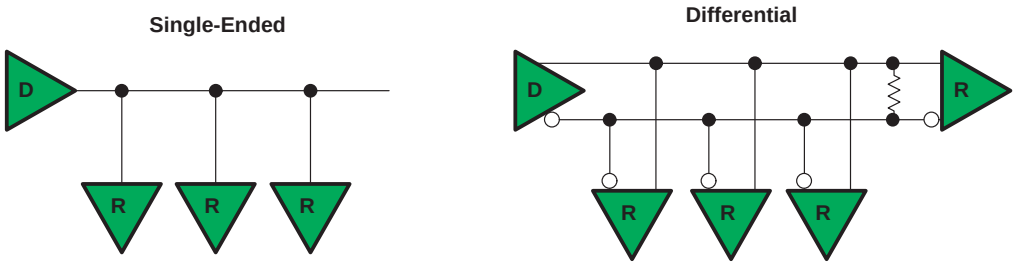


Figure 9. Multi-Drop Connection

Figure 9 shows a topology with only one driver and many receivers.

The next topology is when many receivers and transmitters connect to the same line. In this case, it is called a multi-point configuration.

Multi-Point: This configuration is implemented with many transmitters and many receivers per line. In practice, this solution is normally realized with a transmitter—receiver pair called a transceiver. Not all of the participants have to be transceivers. Any combination of receivers, transmitters and transceivers, is possible for this topology.

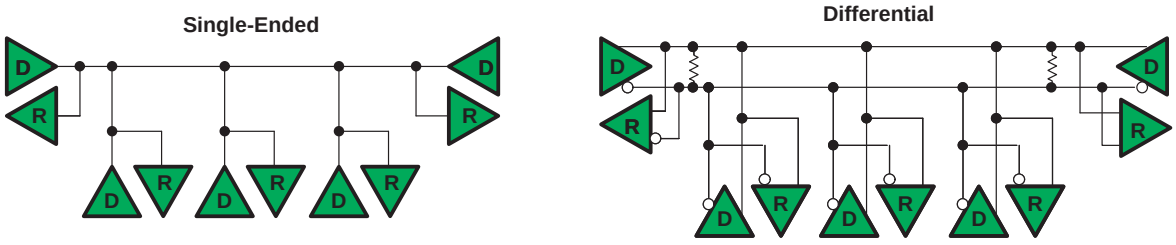


Figure 10. Multi-Point Connection Using Multiple Transceiver

IEEE 1394 Cable and Backplane Applications (FireWire)

1394–1995 is an IEEE designation for a high performance serial bus. This serial bus defines both a backplane (for example, VME, FB+) physical layer and a point-to-point cable-connected virtual bus. The backplane version operates at 12.5, 25, or 50 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps. Both versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol.

The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The 1394 standard also provides new services such as realtime I/O and live connect/disconnect capability for external devices.

Electrical

The 1394 standard is a transaction-based packet technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as 10 bits for bus ID, 6 bits for node ID and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, with each having up to 63 nodes, each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes may physically reside in a single module, and multiple ports may reside in a single node.

Some key features of the 1394 topology are multi-master capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. Another feature is that transmission speed is scalable from approximately 100 Mbps to 400 Mbps.

Each node acts as a repeater, allowing nodes to be chained together to form a tree topology. Due to the high speed of 1394, the distance between each node or hop should not exceed 4.5 m plus the maximum number of hops in a chain which is 16, for a total maximum end-to-end distance of 72 m. Cable distance between each node is limited primarily by signal attenuation. An inexpensive cable with 28-gauge signal pairs can be up to 4.5 meters long. The most widely separated nodes must have 16 or fewer cable hops between them. This gives an end-to-end distance of 72 meter.

A maximum of 63 nodes can be connected to one network. The cable environment uses a twisted three-pair shielded cable and a miniature connector to carry transmit/receive data as well as to source or sink power (between 8 and 40 V_{CC} at no more than 1.5 A). A unique feature of the 1394 cable version is the distribution of power through the cable for operation of the transceiver’s repeating functions even if the node’s power is off.

The cable-based physical interface uses dc-level line states for signaling during initialization and arbitration. Both environments use dominant mode addresses for arbitration. The backplane environment does not have the initialization requirements of the cable environment because it is a physical bus and does not contain repeaters. Due to the differences, a backplane-to-cable bridge is required to connect these two environments.

The signals transmitted on both the cable and backplane environments are NRZ with data-strobe (DS) encoding. DS encoding allows only one of the two signal lines to change each data bit period, essentially doubling the jitter tolerance with very little additional circuitry overhead in the hardware.

Protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 μs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both non-real-time and real-time critical applications on the same bus.

The cable environment's tree topology is resolved during a sequence of events triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all of the information has been gathered on each node, the bus goes into an idle state waiting for the beginning of the standard arbitration process.

An additional feature is the ability of transactions at different speeds to occur on a single device medium (for example, some devices can communicate at 100 Mbps while others communicate at 200 Mbps or 400 Mbps). Use of multispeed transactions on a single 1394 serial bus requires consideration of each node's maximum capabilities when laying out the connections to ensure that the path between two higher-speed nodes is not restricted by a device with lower-rate capabilities.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include: bus state determination, bus access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

Applicability and Typical Application for IEEE 1394

The transmission of data without burdening the host unit creates a huge market for IEEE1394. Not only does the computer-based equipment in private households require an interface solution for the home and home office network, but also the evolving markets of digital broadcasts, interactive services, games, and home shopping requires a high speed network. The introduction of digital set top boxes, which enable the reception of these services, enables the capability to transmit digital data not only to consumer devices like digital TV, but also to PC and storage media. Beside the consumer, PC, and PC peripheral markets, many industrial applications can be covered by IEEE1394.

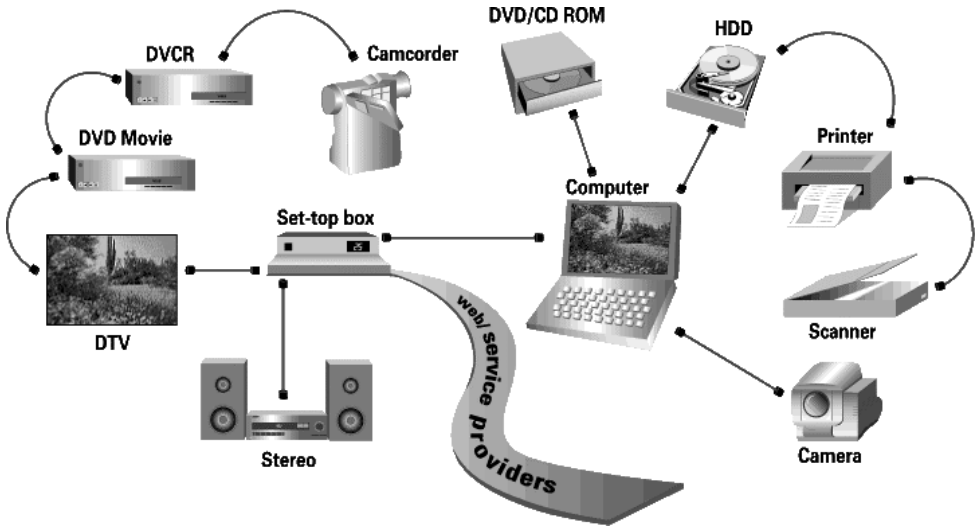


Figure 11. Possible Interconnections Using 1394 as Interface

Applicability and Typical Application for IEEE 1394 Backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, Futurebus+™, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- Diagnostics: Alternate control path to the parallel backplane bus; test, maintenance and troubleshooting; software debug and support interface.
- System enhancement: Fault tolerance; live insertion; CSR access; auxiliary bus to the parallel backplane bus
- Peripheral monitoring: Monitoring of peripherals (disk drives, fans, power supplies, etc. in conjunction with 1394 cable serial bus.

The TSB14C01A and SN74GTLP1394 provide a way to add high-speed 1394 connections to almost any backplane.

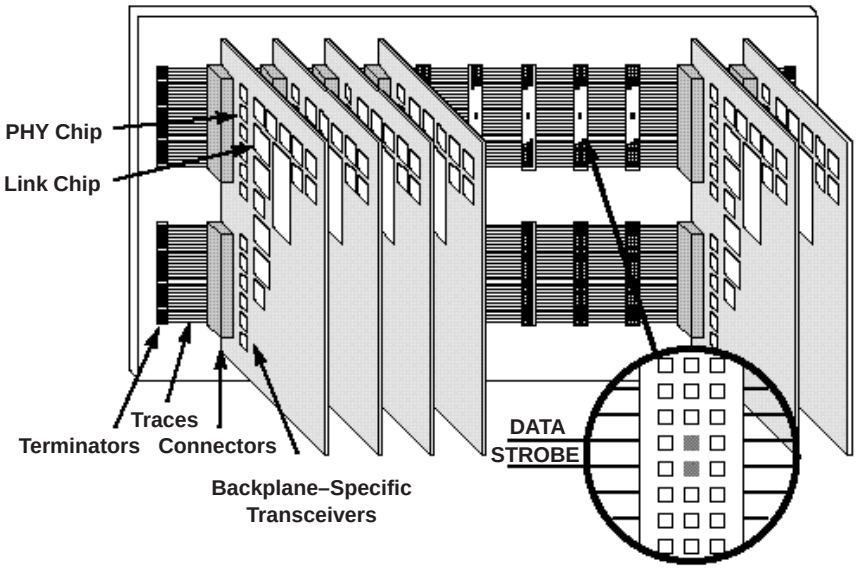


Figure 12. Principle Application Setup Using 1394 Interface

FutureBus+ is a trademark of IEEE, Inc.

Features

- Real-time data transfer for multimedia applications
- 100, 200, and 400 Mbps data rates for high speed applications in cable environments
- 25 and 50 Mbps data rates for backplane environments
- Live connection/disconnection without data loss or interruption
- Automatic configuration supporting plug and play
- Free network topology allowing branching and daisy-chaining
- Guaranteed bandwidth assignments for real-time applications

Table 2. Top IEEE 1394 Link Layer Device List (PC)

DEVICE	SPEED	POWER	PACKAGE
OHCI-Lynx – TSB12LV23	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
PCILynx2 – TSB12LV21B	400 Mbps	3.3 V (5-V tolerance)	176-pin TQFP

Table 3. Top IEEE 1394 Link Layer Device List (Non-PC)

DEVICE	SPEED	POWER	PACKAGE
MPEGLynx – TSB12LV41A	200 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
DVLynx – TSB12LV42	200 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB12LV01A	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
GP2Lynx – TSB12LV32	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP

Table 4. Top IEEE 1394 Physical Layer Device List

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB41LV02	2	400 Mbps	3.3 V (5-V tolerance)	64-pin TQFP
TSB41LV03/04	3/4	400 Mbps	3.3 V (5-V tolerance)	80-pin TQFP
TSB41LV06	6	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB14C01A (Backplane)	x	100 Mbps	5-V	68-pin TQFP

Universal Serial Bus (USB)

Flexibility, expandability, and ease of use are all important in meeting the needs of the growing numbers of PC users. Until now, the traditional PC's peripheral expansion capabilities have largely limited these important user concerns. The new USB standard is an important tool that gives a simple way to expand a system in a virtually unlimited number of ways. Most important, this functionality is available today.

USB is designed to simplify a user's effort by combining the PC's many existing interfaces, like the TIA/EIA-232C serial ports, parallel port, game/MIDI port and more, into a single, easy-to-use connector. In itself, this capability greatly reduces the complexity of the system and gives manufacturers the ability to develop highly integrated products. USB's true plug-and-play capability also signals an end to the often complex process of adding system peripherals.

Electrical

The USB physical interconnect is a tiered star topology. A hub is at the center of each star. Each wire segment is a point-to-point connection between the host and a hub or function, or a hub connected to another hub or function. The USB transfers signal and power over a four-wire cable. The signaling occurs over two wires on each point-to-point segment.

There are two data rates: full-speed signaling bit rate at 12 Mbps and a limited capability low-speed signaling mode at 1.5 Mbps. Both modes can be supported in the same USB bus by automatic dynamic mode switching between transfers. The low-speed mode is defined to support a limited number of low-bandwidth devices, such as a mouse, because more general use would degrade bus utilization. The clock is transmitted, encoded along with the differential data. The clock encoding scheme is NRZI with bit stuffing to ensure adequate transitions. A SYNC field precedes each packet to allow the receiver(s) to synchronize their bit recovery clocks. The cable also carries VBUS and GND wires on each segment to deliver 5 V power to devices.

Protocol

The USB is a polled bus. The host controller initiates all data transfers.

All bus transactions involve the transmission of up to three packets. Each transaction begins when the host controller, on a scheduled basis, sends a USB packet describing the type and direction of transaction, the USB device address, and endpoint number. This packet is referred to as the token packet. The addressed USB device selects itself by decoding the appropriate address fields. In a given transaction, data is transferred either from the host to a device or from a device to the host. The direction of data transfer is specified in the token packet. The source of the transaction then sends a data packet or indicates it has no data to transfer. The destination, in general, responds with a handshake packet indicating whether the transfer was successful.

The USB data transfer model between a source or destination on the host and an endpoint on a device is referred to as a pipe. There are two types of pipes: stream and message. Stream data has no USB-defined structure, while message data does. Additionally, pipes have associations of data bandwidth, transfer service type, and endpoint characteristics like directionality and buffer sizes. Most pipes come into existence when a USB device is configured. One message pipe, the default control pipe, always exists once a device is powered, in order to provide access to the device's configuration, status, and control information.

The transaction schedule allows flow control for some stream pipes. At the hardware level, this prevents buffers from underrun or overrun situations by using a negative acknowledgment handshake to decrease the data rate. When negative acknowledged, a transaction is retried when bus time is available. The flow control mechanism permits the construction of flexible schedules that accommodate concurrent servicing of a heterogeneous mix of stream pipes. Thus, multiple stream pipes can be serviced at different intervals and with packets of different sizes.

Applicability and Typical Applications

USB is a PC-centric system designed to interconnect up to 127 peripherals to the PC including the ones pictured below: keyboard, mouse, printer, modem, etc. Due to the tiered star topology, a hub is needed at the center of each star.

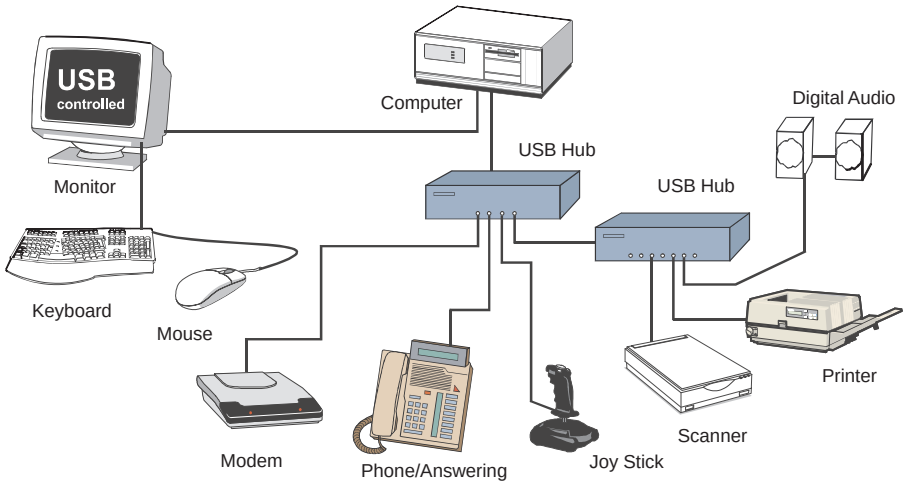


Figure 13. USB – Tiered Star Topology

Features

- Single PC supports up to 127 devices
- Data rates of 1.5 Mbps and 12 Mbps supported
- Ends confusion of multiple add-in cards for ease of use
- Universal connectors and cables for all devices and applications
- Auto configuration upon connection for real plug and play
- Guaranteed bandwidth for real-time applications

Table 5. Top USB HUB Device List

DEVICE	DOWNSTREAM PORTS	POWER	PACKAGE
TUSB2046/43	4	3.3 V	32-pin LQFP
TUSB2077	7	3.3 V	48-pin LQFP
TUSB2140B + I2C	4	3.3 V	40-pin DIP or 44-pin TQFP

TIA/EIA-232

RS is the abbreviation for recommended standard. Usually, it is based on or is identical to other standards, e.g., EIA/TIA-232-F. The following section gives a closer view of these specifications, their benefits, and applicability. Where appropriate, the protocol is briefly described.

TIA/EIA-232, previously known as RS-232 was developed in the 1960's to interconnect layers of the interface (ITU–T V.11), but also the pignut of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC-serial-mouse utilizes only RI, TD, RD and GND). Although the standard supports only low speed data rates and line length of approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

Electrical

TIA/EIA-232 has high signal amplitudes of ±(5 V to 15 V) at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than –3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/µs. The intention here is to limit any reflections that can occur to the rise- and fall-times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary. Due to the voltage swings of –5...15 to 5...15 V a dual supply voltage was necessary in the past. Nowadays many devices operate with single supplies, generating the large positive and negative driver output voltage swings with integrated charge-pumps.

Protocol

Different from other purely electrical-layer-standards, TIA/EIA-232 defines not only the physical layer of the interface (ITU-T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ITU-T V.24). The interface standard specifies also handshake and control lines in addition to the 2 unidirectional receive data line (RD) and transmit data line (TD). The control lines might be used, but do not necessarily have to be.

Applicability

TIA/EIA-232 is historically associated with computers interfacing with peripherals at low speed, short distance, for example, mouse, modem, joystick, etc., or to interconnect two PCs (that is, null modem, Figure 14). Today other equipment also uses TIA/EIA-232 I/O, for example, for programming purposes.

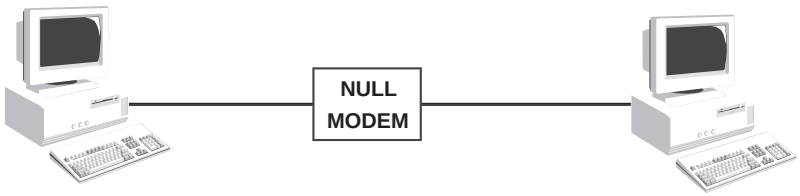


Figure 14. Null Modem Application Using RS232

Features

- Established standard
- Inexpensive
- Universally used

Table 6. Top TIA/EIA-232 Device List

DEVICE	BIT WIDTH	POWER	ESD PROTECTION	PACKAGE
SN74LP1185	3 drivers/ 5 receivers	V_{CC}: 5 V, 12 V, and –12 V I/O: LVTTL/.RS-232	±15 kV HBM ESD (on bus pins)	20-pin PDIP, SOIC SSOP, and TSSOP
SN85LPE185	3 drivers/ 5 receivers	V_{CC}: 5 V, 12 V, and –12 V I/O: LVTTL/.RS-232	±15 kV HBM ESD (on bus pins)	20-pin PDIP, SOIC SSOP, and TSSOP
SN75LP196	5 drivers/ 3 receivers	V_{CC}: 5 V, 12 V, and –12 V I/O: LVTTL/.RS-232	±15 kV HBM ESD (on bus pins)	20-pin PDIP, SOIC SSOP, and TSSOP

TIA/EIA-422

TIA/EIA-422 (RS-422) allows a multi-drop interconnection of one driver, transmitting unidirectionally to up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

Electrical

TIA/EIA-422 (ITU-T V.11) is comparable to TIA/EIA-485. It is limited to unidirectional data traffic and is terminated only at the line-end opposite to the driver (please refer to the multi-drop-explanation at the beginning of this report). The maximum line length is 1200m, the maximum data rate is determined by the signal rise- and fall-times at the receiver's side (requirement: <10% of bit duration) and ends up to be approximately 10 Mbps. TIA/EIA-422 allows up to ten receivers (input impedance of 4 kΩ attached to one driver. The maximum load is limited to 80 Ω. Although any TIA/EIA-485 transceiver can be used in a TIA/EIA-422 system, dedicated TIA/EIA-422 circuits are not feasible for TIA/EIA-485, due to short circuit current limitations. The TIA/EIA-422 standard requires only short circuit limitation to 150 mA to ground, while TIA/EIA-485 additionally has to limit short circuit currents to 250 mA from the bus pins to –7 V and 12 V to address malfunctions in combination with ground shifts.

Protocol

Not applicable/none specified

Applicability

TIA/EIA-422 is very often used in industrial areas due to its robustness. Compared to TIA/EIA-485, it can only control without receiving any feedback from the listeners since its transmission mode is multi-drop, meaning only one driver is attached to a bus with multiple receivers. Backplane applications are often realized with a TIA/EIA-422 physical layer.

Features

- Established standard
- Good for multi-drop over long distances
- Good for use in noisy environments
- Wide temperature range: –40°C to 85°C – suitable for industrial applications

Table 7. Top TIA/EIA-422 Device

DEVICE	BIT WIDTH	POWER	PACKAGE
AM26LS31	4 drivers	V_{CC}: 5 V I/O: (LV)TTL/RS-422	16-pin PDIP and SOIC
AM26LS32A	4 receivers	V_{CC}: 5 V I/O: (LV)TTL/RS-422	16-pin PDIP and SOIC
SN75ALS192	4 drivers	V_{CC}: 5 V I/O: (LV)TTL/RS-422	16-pin PDIP and SOIC

TIA/EIA-485

Historically, TIA/EIA-422 was on the market before TIA/EIA-485. Due to the lack of bidirectional capabilities, a new standard adding this feature was created: TIA/EIA-485 . The standard (TIA/EIA-485-A or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above and line lengths of up to 1200 m. Of course both limits can not be reached at the same time. Furthermore, recommendations are given regarding wiring and termination. The specification does not give any advice on the connector or any protocol requirements.

Electrical

TIA/EIA-485 describes a half-duplex, differential transmission on cable lengths of up to 1200 m and at data rates of typically up to 35 Mbps (requirement similar to TIA/EIA-422, but tr<30% of the bit duration, there are also faster devices available, suited for higher rates under certain load-conditions). The standard allows a maximum of 32 unit loads of 12 kΩ, equal to 32 standard nodes or even higher count with increased input impedance. The maximum total load should not drop below 52 Ω. The common-mode voltage levels on the bus have to maintain between –7 V and 12 V. The receivers have to be capable to detect a differential input signal as low as 200 mV.

Protocol

Not applicable/none specified; exceptions: SCSI systems (please refer to appropriate section) and the DIN-Bus DIN66348

Applicability

Due to the robustness against noise because of the differential transmission mode and to ground shifts achieved by the large common mode voltage range, this standard is perfectly suited for industrial applications. The data rate is usually sufficient, e.g., to control a process line. TIA/EIA-485 is also very widely used for backplanes (e.g., telecom applications) since the high node-count and data-integrity are necessary features for these applications.

Features

- Very robust interface (common mode range: –7 V to 12 V) – suitable for industrial applications
- Wide temperature range: –40°C to 85°C – suitable for industrial applications
- Up to 64 nodes with the SN75LBC184

Table 8. Top TIA/EIA-485 Device List

DEVICE	BIT WIDTH	POWER	PACKAGE
SN75LBC184	1 Ch	V_{CC}: 5 V I/O: (LV)TTL/RS-485	8-pin SOIC
SN75LBC176	1 Ch	V_{CC}: 5 V I/O: (LV)TTL/RS-485	8-pin SOIC
SN75ALS176	1 Ch	V_{CC}: 5 V I/O: (LV)TTL/RS-485	8-pin SOIC

SCSI

Small computer systems interface (SCSI) has been developed in order to interconnect computers and its peripherals with a high data throughput. The first standard described a single ended interconnection. The next generation was high voltage differential – small computer systems interface (HVD-SCSI), which uses TIA/EIA-485 as the physical layer. Low voltage differential – small computer systems interface (LVD-SCSI) standard has been evolved to address even higher data rates.

Electrical

Electrically, HVD-SCSI is identical to TIA/EIA-485 (please refer to the TIA/EIA-485 section for details). The maximum line length is reduced to 25 m at 20 Mbps or 12 m at 40 Mbps. Details can be found in the ISO/IEC 9316 Standard: *Information technology, Small Computer System Interface-2*.

Single ended SCSI operates on TTL-levels and supports data rates up to 10 Mbps. LVD-SCSI is a newer standard with electrical levels similar to TIA/EIA-644 or LVDS (please refer to the appropriate section). It supports transmission speeds up to 40 Mbps on 12 m length, but 80 Mbps and even 160 Mbps are targeted with the upcoming specifications. Furthermore, the EMI of LVD-SCSI is reduced by approximately 90% compared to single-ended SCSI and the power consumption is at about 20% of HVD-SCSI. The maximum number of nodes including the host/controller is eight. A separate control bus, consisting of nine lines, is necessary for synchronization, arbitration, and addressing purposes. Furthermore, a parity bit is added to the 8-bit data bus. Wide SCSI utilizes an additional 8 (+1 parity) bit data bus to transfer a 16 bit wide SCSI word.

Protocol

The SCSI protocol is also defined in the ISO/IEC 9316 Standard: *Information Technology, Small Computer System Interface-2*. All commands as well as pin assignments are specified therein. Timing and arbitration are also described. As the standard is very voluminous, it is out of the scope of this report to get into details. For further information please refer to the mentioned standard.

Applicability and Typical Application

SCSI is suited for the interconnection of equipment transferring a high amount of data in a parallel mode (byte, double, 32-bit wide). Therefore, nowadays it is primarily used in the computer domain to interconnect a host (computer) with its peripherals (printer, scanner, hard disks, CD-RW, etc). Recently, manufacturers of other hardware, which requires a high data throughput, have explored the advantages of SCSI as well. The node-limit of eight is sometimes not sufficient, but the limit can be exceeded in proprietary systems.

Features

- Established standard
- Can migrate from single-ended SCSI to HVD and then LVD

Table 9. Top SCSI Device List

DEVICE	BIT WIDTH	POWER	PACKAGE
SN75976	9 Ch HVD SCSI	V_{CC}: 5 V I/O: (LV)TTL/HVD-SCSI	56-pin SSOP or 56-pin TSSOP
SN75LVDM976	9 Ch LVD or SE-SCSI	V_{CC}: 5 V I/O: (5 V) CMOS/LVD/SE-SCSI	56-pin TSSOP

TIA/EIA-644 (LVDS)

Low voltage differential signaling (LVDS) is an approach to achieve higher data rates on commonly used media. Since the limitation of the previously known differential standards is mainly related to the maximum achievable slew rate and EMI restrictions, the new development targets low voltage swings that will be reached much faster, even while the slew rate remains the same. In this way, in addition to enabling higher speeds, EMI, as well as power assumption, is reduced.

Electrical

As the name says, LVDS utilizes differential transmission mode and low signal amplitudes. The swing is in the range of only 300 mV, generated on a 100 Ω-termination resistor. The driver is actually a current mode driver forcing an output current between 2.47 mA and 4.54 mA into either one of the two outputs. This way, the device is always drawing the same supply current and eliminates almost any feedback to the supply. In comparison, a voltage mode driver (like used for TIA/EIA-422) pulls much higher current during the switching period than in the steady state. The chart below shows the dependency of the supply current versus the switching frequency. As can be seen, the supply current is significantly lower and also the increase over frequency is much lower with the use of LVDS drivers.

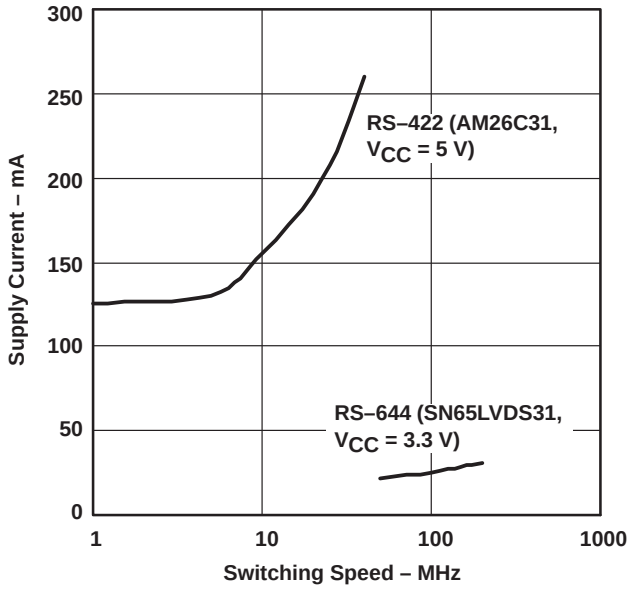


Figure 15. Supply Current Versus Switching Frequency

The standard allows up to 655 Mbps. The maximum line length is not specified. 15 m is given as a recommendation. The specification addresses only point-to-point interfaces, but it allows the attachment of multiple receivers if attention is paid to several conditions. These include stub line length, termination, and signaling rate.

Protocol

There is no protocol specified for TIA/EIA-644. This is left to the user/hardware designer.

Applicability

LVDS targets applications that transfer data point-to-point at very high speeds. It is also capable of driving multiple receivers if care is taken regarding the load configuration (that is, it can be used as a TIA/EIA-422 replacement, if certain conditions are met.) LVDS is particularly suitable for any application that requires low power and/or low EMI. The common mode input voltage, which is currently limited to 0 V to 2.4 V, restricts the usage of LVDS with long line lengths causing unpredictable ground shifts as well as the use in electrically noisy environments.

Features

- Very high speed
- Very low power consumption
- Very low EMI
- Low cost
- Same pinout as existing TIA/EIA-422 and TIA/EIA-485 Parts

Table 10. Top LVDS Device List

DEVICE	BIT WIDTH	POWER	PACKAGE
SN65LVDS31/32	400 Mbps	V_{CC}: 3.3 V I/O: LVTTL/.LVDS	16-pin SOIC
SN65LVDS179	400 Mbps	V_{CC}: 3.3 V I/O: LVTTL/LVDS	8-pin SOIC

LVDM

LVDM stands for LVDS-multi-point, enabling a half-duplex operation with LVDS voltage levels and speeds. It benefits from the same advantages as LVDS, additionally it allows bidirectional data transfer and the attachment of several drivers, receivers, and/or transceivers.

Electrical

LVDM is LVDS with doubled driver output current. Due to the bidirectional transfer capability, a line termination is needed at each end. The requirement of termination matching the line impedance remains. Therefore, both ends are terminated with 100 Ω. The effective termination resistance will result in the parallel configuration of these two resistors, equaling half the impedance or twice the load. To ensure the same input voltage levels like with LVDS at a 100-Ω load, the output current is doubled to generate the required amplitude on just 50 Ω.

Protocol

Not applicable/none specified.

Applicability

LVDM can be used as a replacement for TIA/EIA-485 interconnections, especially for high speed, low power and/or low EMI interfaces. Like LVDS, the common mode input range is between 0 V and 2.4 V which limits the line length and the applicability in a electrically noisy environment. It is suited for backplane applications and cabled interfaces.

Features

- Very high speed
- Very low power consumption
- Very low EMI
- Low cost
- Same pinout as existing TIA/EIA-42 and TIA/EIA-485 parts

Table 11. Top LVDM Device List

DEVICE	BIT WIDTH	POWER	PACKAGE
SN65LVDM176	400 Mbps	V_{CC}: 3.3 V I/O: LVTTL/LVDS	8-pin SOIC
SN65LVDM050	400 Mbps	V_{CC}: 3.3 V I/O: LVTTL/LVDM	16-pin SOIC

LVDS Serdes and FlatLink

LVDS serializer deserializer (serdes) and FlatLink technology based devices physically interconnect two parallel bus systems through a high frequency serial data path using LVDS technology. The following explanations apply to both, LVDS serdes and FlatLink type devices; differences are mentioned in the text accordingly.

Principle of a Serdes (serializer/deserializer) Device: The requirement for functionality is a transmitter and a receiver. From a user standpoint, the application is doing nothing more than repeating a number of parallel-clocked data over a longer distance. Therefore, the receiver's output appears to the user the same as the signal seen on the transmitter's input bus. The range for the bus clock rate is limited (e.g., 31–65 MHz).

The transmitter has a certain number of LVTTL compatible data input pins (parallel bus) and a clock input. The input pins are split up into different groups. All of the data signals in one group become serialized into a higher frequent data stream and sent out over differential lines (LVDS). A typical compression value is 1:7. The process can be compared with a multiplexer which is switching between all signals of a group running on a frequency equal to the clock multiplied by the number of pins in this group. This serial data stream is sent into a differential pair of lines based on LVDS. The original clock signal is transferred over an additional pair of lines.

On the receiving side, the high frequency differential data stream is demultiplexed separately for each group (each differential input) and clocked out to the parallel LVTTL compatible output bus.

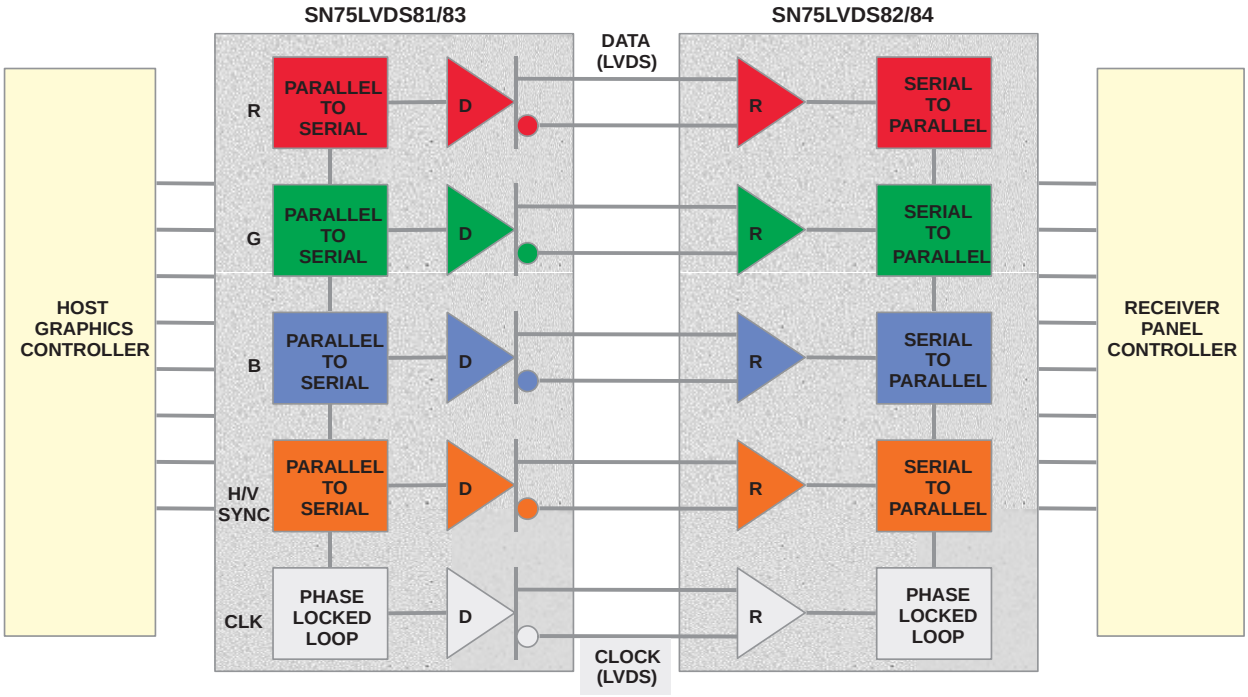


Table 12. Typical Multiplexing Ratio for Serdes Devices

Transmitter	Input (LVTTL): Output (LVDS serial link):	21 lines + clock 3 lines + clock
Receiver	Input (LVDS serial link): Output (LVTTL):	3 lines + clock 21 lines + clock

Electrical

No industrial standard covering LVDS serdes or FlatLink devices has been defined so far.

The I/O Bus pins are LVTTL compatible. The transmission is based on LVDS. All devices meet or exceed the ANSI EIA/TIA-644 Standard that specifies LVDS. LVDS serdes devices are designed for the industrial temperature range (–40°C to 85°C) running on a single 3.3 V power supply. Depending on the transmission frequency, the transmission media, and the environment (noise level), LVDS serdes supports a transfer distance of up to 16 meter.

Protocol

No protocol is specified for LVDS serdes or FlatLink; this is left to the user/hardware designer.

Applicability

FlatLink: is designed to transfer large data packets from the CPU to the graphic LCD display in a notebook type of application. The major advantages compared with realizing this transfer based on standard bus logic are in reduced number of parallel data lines, reduced power consumption, and lower electromagnetic emission.

LVDS Serdes: The differential transmission mode provides high robustness against in-coupling noise. Therefore, LVDS serdes devices are perfectly suited to industrial applications, as point-to-point connection in telecom backplanes, or to interconnect two parallel bus systems.

Bus speed: The clock rate of those bus systems must be chosen within a defined range. The limiting factor for minimum and maximum clock speed is the PLL of the transmitter that needs to lock to the clock input. Test of devices specified for 31 MHz to 65 MHz clock input have shown that they work down as low as 10 MHz at room temperature and the highest data rate is slightly above 65 MHz.

Bus skew: The output data clock of the serdes receiver is a device specific parameter, independent of the input bus skew. This might help to overcome bus skew problems.

Bus Topology: Serdes can be used as point-to-point or multi-drop connections as well as replacing slower bus systems via a daisy chaining architecture.

Initialization after reset/power down: As typical in all PLL based applications, the receiver requires a certain time to lock to the clock signal. Therefore, the result on the receiver output becomes valid after a duration of 1 ms.

Figure 16. Typical Application – FlatLink Used as an Interface in a Notebook

Features

- PLL lock range 31–65 MHz (speed for parallel input bus
- Data throughput up to 455 Mbps over each differential pair
- Industrial temp spec (–40°C to 85°C for LVDS serdes
- Very low power consumption and low emission (portable devices)
- Cost per Mb transfer rate very low (1.1 Cent)
- Very low power consumption when disabled (below 1 mW)
- Easy hardware implement of parity proof, due to high number of parallel inputs

Table 13. Top LVDS Serdes Device List

DEVICE	Serdes Ratio	MAXIMUM THROUGHPUT	V_{CC} AND I/O	PACKAGE
LVDS serdes				
SN65LVDS93/94	28:4	1.365 Gbps	3.3 V Parallel I/O: LVTTL Serial I/O: LVDS	56-pin TSSOP
SN65LVDS95/96	21:3	1.8 Gbps	Power supply: 3.3 V Parallel I/O: LVTTL Serial I/O: LVDS	48-pin TSSOP
FlatLink				
SN75LVDS84A/ SN75LVDS86A	21:3	1.8 Gpbs	85 mW typical (84A) 145 mW typical (86A)	48-pin TSSOP

Serial Gigabit CMOS

The product family of gigabit serdes devices has been made to bridge large number of data bits over a small number of data lines. The input to the transceiver is a parallel bus system, bit wide (n=1,2,4,8), with a clock speed in the 100 MHz range. This input bus signal will be serialized and sent over a differential pair of cable to the second transceiver which recovers (de-serializes) the bus pattern and clocks it out in parallel. Input and output bus appear identical to the user.

Serial gigabit CMOS products address primary point-to-point high-speed data transfer applications.

Electrical

Ultra high-speed serdes devices are compliant to the IEEE802.3z gigabit ethernet standard defined by the IEEE P802.3z gigabit task force. This standard specifies the physical and the data link layer (in reference to the OSI model) for a serializer/deserializer device running up to 1 Gbps throughput. The model is split into 6 main tasks as it is logical link control (LLC), media access control (MAC), reconciliation, physical coding sublayer (PCS), physical medium attachment (PMA), and physical layer medium dependent (PMD). The definitions are made to be inline with the gigabit media independent interface (GMII) transmission standard, defining signal functions for a interface up to 1 Gbps. TI extended this standard to GMII-2 with the same terminology but effective data throughput up to 2 Gbps.

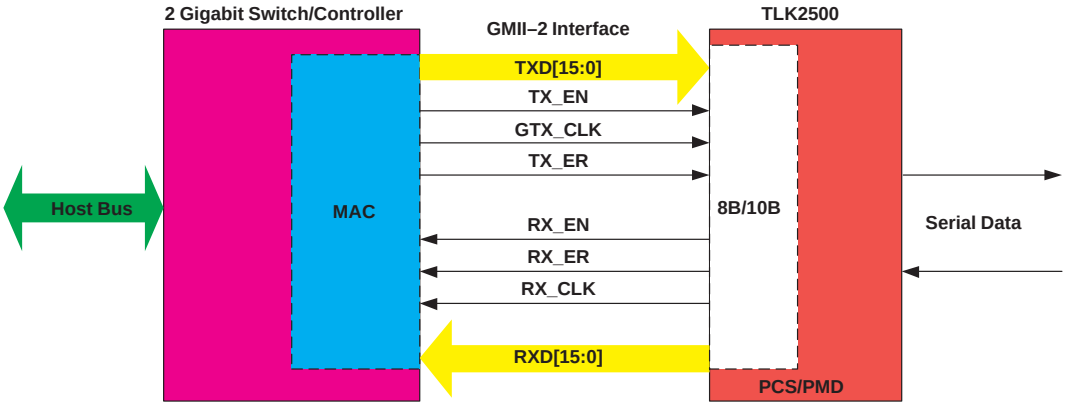


Figure 17. GMII-2 Interface

Parallel I/O side: V_{CC} ±0.3 V.

Serial (transmission) side: The driver design on the serial side is not specified in the IEEE802.3z. Texas Instruments is using high-speed current mode logic (CML) technology. With a typical logic swing of 400 mV and input sensitivity of 200 mV this technology provides sufficient noise margin for most applications. The CML interface is chosen for:

1. Low power consumption
2. High noise immunity
3. Ease of defining logic swing at the receiver
4. Inherently short circuit proof

5. Simpler level shifting to CMOS levels
6. Adjustable logic swing can save power over short connections

The following steps will be performed on the transmitter side:

1. The incoming bus signal will be buffered in reference to the input clock signal
2. 8B10B encoding of the data word (this ensures clock recovery on the receiver side due to a high transition rate of equal/above 3+1 transitions on 8 bit data)
3. Serialization of the data
4. Clock the serial data into the differential line using the CML driver

The receiver side performs the reverse operations in reverse order to regenerate to original sent word.

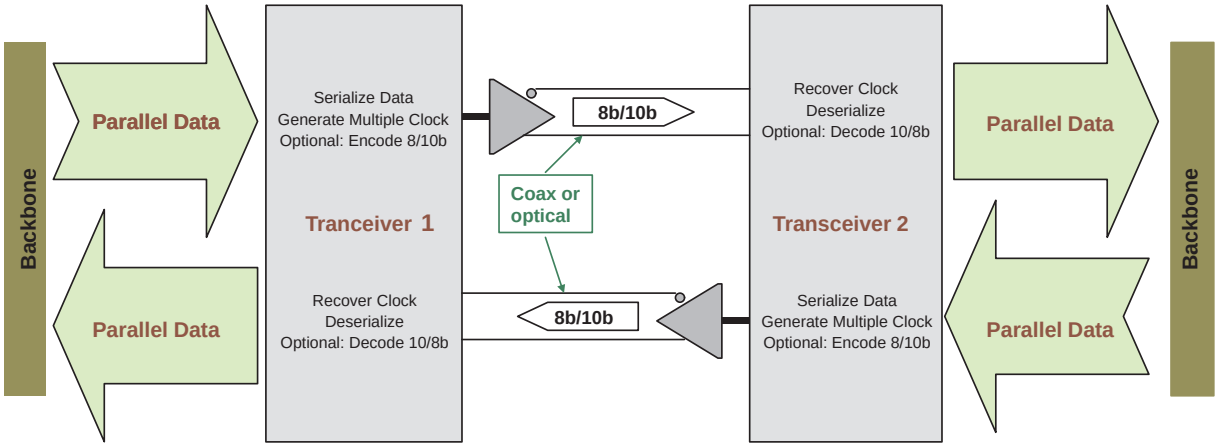


Figure 18. Serdes Interface Using Two Transceivers

Transmission media: The transmission media of the serial path can be PCB, copper cable, or fiber-optics using an electrical-to-optical translator circuit in-between. The impedance of the copper must be matched to 50 (75) Ω. The maximum distance to be bridged depends on the transmission speed and the transmission media; tests showed proper functionality up to 5 m over coax cable.

Protocol

There is no protocol specified for IEEE802.3z. This is left to the user/hardware designer. The upper 5 layer (application, presentation, session, transport and network) of the OSI reference model are left open to be used application-specifically.

Applicability

The differential transmission mode provides high robustness against in-coupling noise. Therefore, serdes devices suit perfectly into networking, telecommunication, or data-communication designs or to interconnecting two parallel bus systems.

Bus speed: The clock rate of those bus systems can be chosen within a certain range (e.g., 80–125 MHz). The limiting factor on minimum and maximum clock speed is the PLL on the receiver side, which has to recover the clock out of the serial data stream.

Bus skew: The output data clock of a gigabit series device is device specific and independent of the input bus skew. This might help to overcome bus skew problems.

Bus Topology: Series can be used as point-to-point connection as well as replacing slower bus systems via a daisy chain architecture.

Initialization after reset/power down: As typical in all PLY based applications, the receiver requires a certain time to lock to the incoming serial signal. Therefore, the receiver output and control pins are kept into a high-impedance state that could take one millisecond.

Receive Interface – data alignment (8B/10B encoding): The receiver has a state machine implemented to detect the boundary of the data word out of a continuous serial bit stream. Special carrier words and an initialization algorithm after reset or data loss ensure correct data transfer. Control outputs on the receiver inform the user about the actual transmission state as it can be normal data transfer, transmission error, idle, or carrier extension.

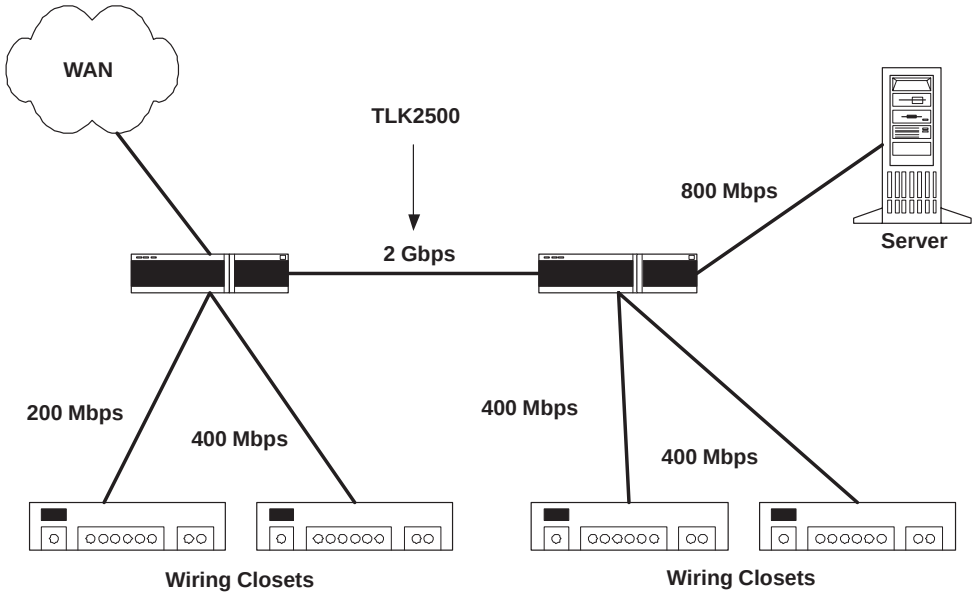


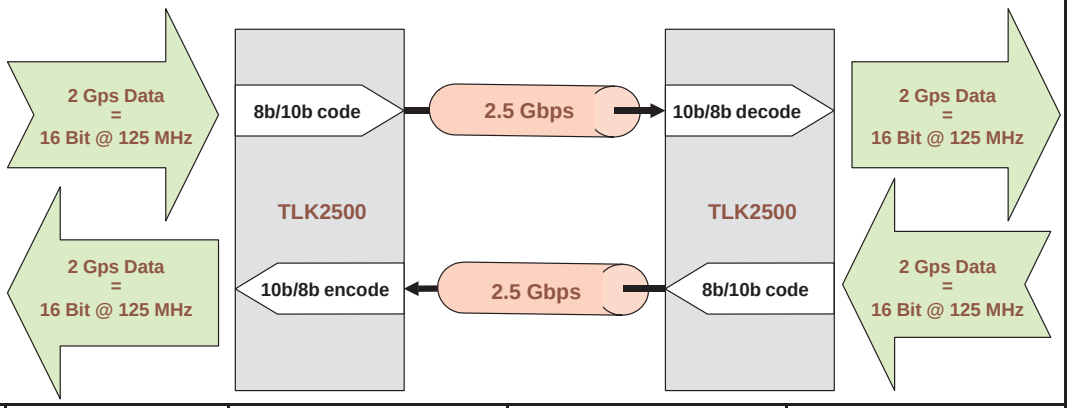
Figure 19. High-Speed Interface Using TLK2500

Features

- Data throughput up to 2 Gbps over each differential pair
- Differential line driver with adjustable voltage swing; advantage: optimized for a particular transmission line impedance and length, as well as for controlling the output swing for EMU and attenuation concerns
- Very low power consumption, low emission
- Using a daisy chain layout offers multi-drop architecture
- Very low output jitter (40 ps)
- External pin signalizes data errors on receiving side
- Clock recovery

- TX/RX full duplex
- Optional: device built-in self test and bus test using a device internal random bit generator

Table 14. Top Serial Gigabit Device List

DEVICE	Series Ratio	THROUGHPUT (Gbps)	V_{CC} AND I/O	PACKAGE
TNETE2201A (Gigabit ethernet transceiver)	10:1 Receiver expects 8B/10B coded data	1.25	3.3 V CMOS 5 V tolerant Serial I/O: PECL	64-pin QFP
TLK2201 (Gigabit ethernet transceiver)	10:1 Device expects 8B/10B coded data	1.0 – 1.6	V_{CC}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: CML	RCP64 (VQFP)
TLK2500	16:1	1.6 – 2.5	V_{CC}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: CML	RCP64 (VQFP)
				
TLK2514 (product preview)	4 × 16:1	4 * 3.2	as above	257-pin BGA

PCI/CompactPCI

The primary goal of the PCI developers was a low cost, flexible, high performance industry standard local bus architecture. To enable portable systems with PCI bus, low power dissipation also was a requirement. Personal computers have been the first area where the PCI became the standard for local busses. Meanwhile the PCI bus starts to become a major player in the industrial area. For industrial applications the form factor changed to CompactPCI and hot-swap has been included. The PCI Special Interest Group (PCI SIG: http://www.pcisig.com) maintains the specifications of the PCI bus and the PCI Industrial Computer Manufacturers Group (PICMG: http://www.picmg.org/) takes care of the CompactPCI specification.

Electrical

- 32-bit address space
- 32 or 64-bit data path
- 33 MHz and 66 MHz bus clock speed
- Maximum data rate:
  - 1 Gbps for 33 MHz/32-bit bus; 4 Gbps for 66 MHz/64-bit bus
- Two major form factors:
  - Personal Computer: 62 pin connector for 32-bit (Figure 20) and 82 pin connector for 64-bit systems.
  - CompactPCI: Eurocard industry standard, both 3U (100 mm by 160 mm) and 6U (233.35 mm by 160 mm) board sizes (Figure 21)
- CMOS drivers; TTL voltage levels
- 5 V, 3.3 V interoperable
- Reflected wave switching, thus the bus is short. To increase the number of connected devices PCI-to-PCI bridges are necessary. Figure 22 shows a PCI system with 8 PCI busses.
- Direct drive – no external buffers

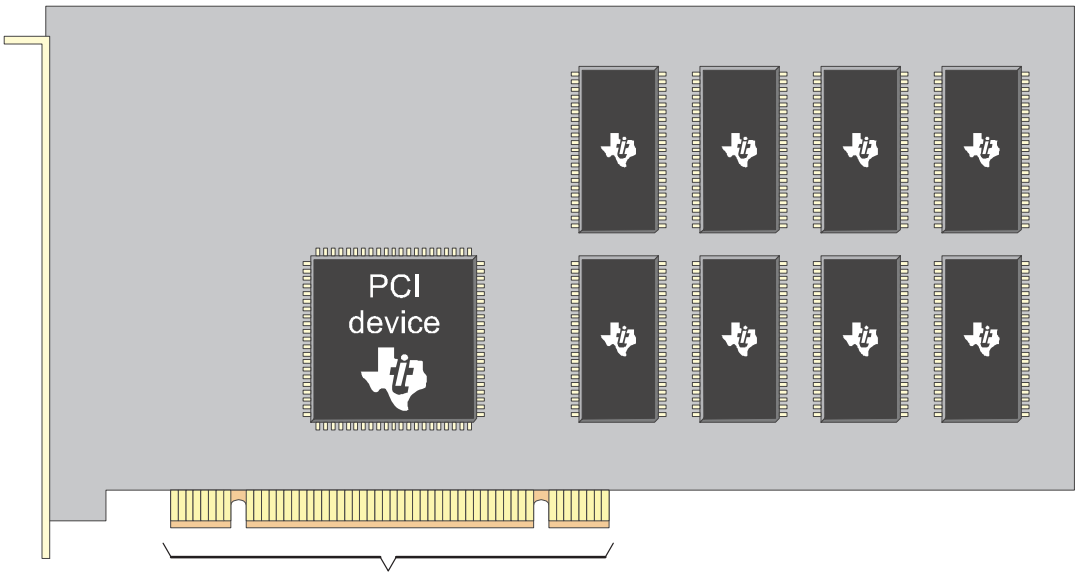


Figure 20. PCI Card for Personal Computer

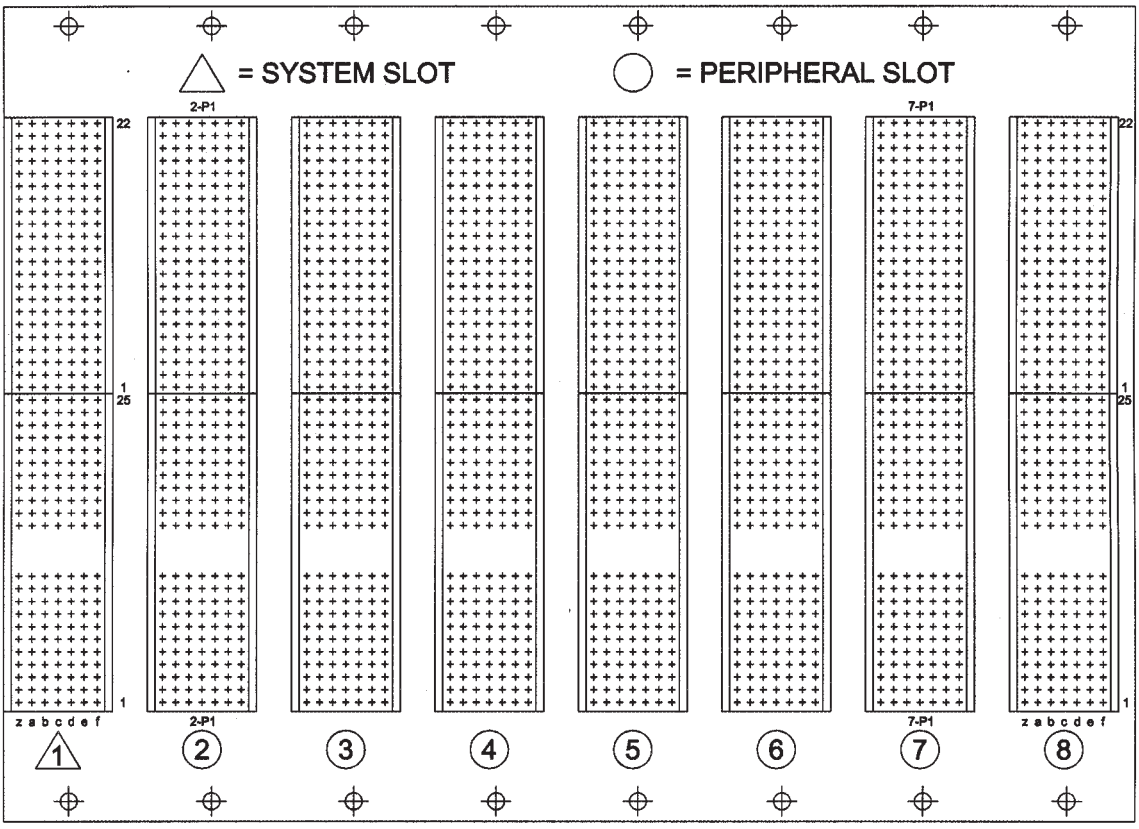


Figure 21. CompactPCI Backplane

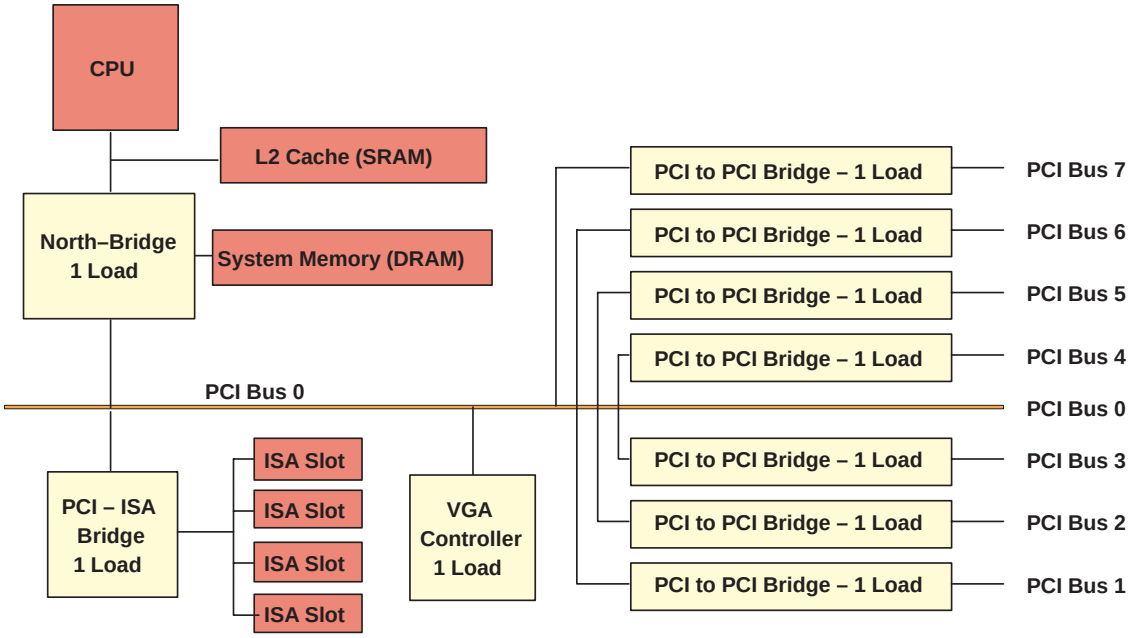


Figure 22. PCI Bus System With 8 PCI Buses

Protocol

Initialization

PCI devices are not configured after the supply power is switched on. None of the devices have a memory or address range assigned, and no interrupts are available. To operate a PCI bus, all connected devices (master and slaves) have to be configured. Through the configuration space the controller reads the requirements of a device and is able to assign memory-, I/O-space and Interrupts. This enables plug-and-play systems.

In large systems with multiple PCI busses, the configuration software needs an enumerator to number all busses in the system and to program the PCI-to-PCI bridges accordingly.

Operation

During operation each device on the bus may become the master and can transfer data to any other bus member. The bus design requires burst transfers to work efficiently. Still single byte transfers are still possible.

Applicability

The PCI bus is a computer bus system. The first and biggest success was the personal computer. Nearly every system in the world is equipped with a PCI bus system. High data rates, low cost, multi-media support, and scalability have been key features of the PCI bus that led to the success.

Notebook computers make advantage of the low-power consumption. The reflected wave switching design does not require any termination or additional bus-drivers. The disadvantage is a short bus length that can be increased using PCI-to-PCI bridges. Notebook docking stations often use PCI-to-PCI bridges to generate a new PCI bus in the docking unit.

In the industrial area CompactPCI gains more and more market share. CompactPCI comes in a Eurocard industry standard rack and supports hot-swap. According to the requirements of the industrial environment, high quality connectors with hot-swap support are used for CompactPCI. Besides hot-swap capabilities, the electrical specifications and protocols are identical to PCI. Especially in Telecom and server applications 66 MHz and 64-bit systems are used.

Features

- Processor independent
- Multi-master; peer-to-peer
- Supports memory, I/O, and configuration space
- Data bursting as normal operation mode—both read and write—variable burst length
- Low latency guarantees for real-time devices
- Initialization hooks for auto-configuration
- Arbitration: central,k access oriented, and hidden
- 64-bit extension transparently interoperable with 32-bit

Table 15. Top Device List – PCI Products

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
PCI1410	PCI 2.2	PCI to CardBus bridge for one cardbus slot	144-pin LQFP 144-pin BGA CSP	Available
PCI1420	PCI 2.2	PCI to CardBus bridge for two cardbus slots	208-pin LQFP 209-pin BGA CSP	Available
PCI1450	PCI 2.2	PCI to CardBus bridge for two cardbus slots and integrated zoom-video support	256-pin LQFP 256-pin BGA 257-pin BGA CSP	Available
PCI4450	PCI 2.2	PCI to CardBus/1394 bridge for two cardbus slots, integrated zoom-video support	256-pin BGA 257-pin BGAS CSP	Available
PCI2031	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33 MHz, 6 secondary master	176-pin LQFP	Available
PCI2250	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33 MHz, 4 secondary master	160-pin LQFP 176-pin LQFP	Available
PCI2050	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33 MHz, 9 secondary master	208-pin LQFP 209-pin BGA CSP	Available
PCI2040	PCI 2.2	PCI-to-DSP bridge	144-pin LQFP 144-pin BGA CSP	Available
PCI2450	PCI 2.2	PCI-to-PCI bridge, 64-bit, 66 MHz, 9 secondary master	304-pin BGA	Available

IEEE 1284 Compatible Devices (SN74yyy1284)

The IEEE 1284 standard provides an open path for communication between computers and intelligent printers and peripherals. The release of the standard signaling method for a bidirectional parallel peripheral interface for personal computers defines a common standard for bidirectional parallel communications between personal computers and peripherals. Preexisting methods used a wide variety of hardware and software products, each with unique and—in most cases—incompatible signaling schemes. As an example the centronics printer port shall be mentioned. There has never been an official standard for this printer port. Therefore problems in circuit designs occurred due to unknown hardware design elements, such as termination resistors or driver output impedance. For safe data transmission, only a short cable between host and peripheral (1 to 2 m) was acceptable. The release of the IEEE1284 standard answers the demand for an industry-wide, high-speed, high-integrity parallel port standard for a bidirectional peripheral interface. Texas Instruments offers three bus drivers. They support reliable data transfer via cables lengths up to 10 meter (30 feet) at a speed of 16 Mbps.

Electrical

The IEEE1284 specification defines the physical set-up of the 1284—interface including wiring diagram, minimum drive capabilities and termination considerations.

Protocol

The protocol is defined in the IEEE1284 standard.

Applicability

The ’1284 compatible devices are widely used from computer and peripheral manufacturers, because the ’1284 standard can communicate more than 50 times faster than conventional parallel port interfaces.

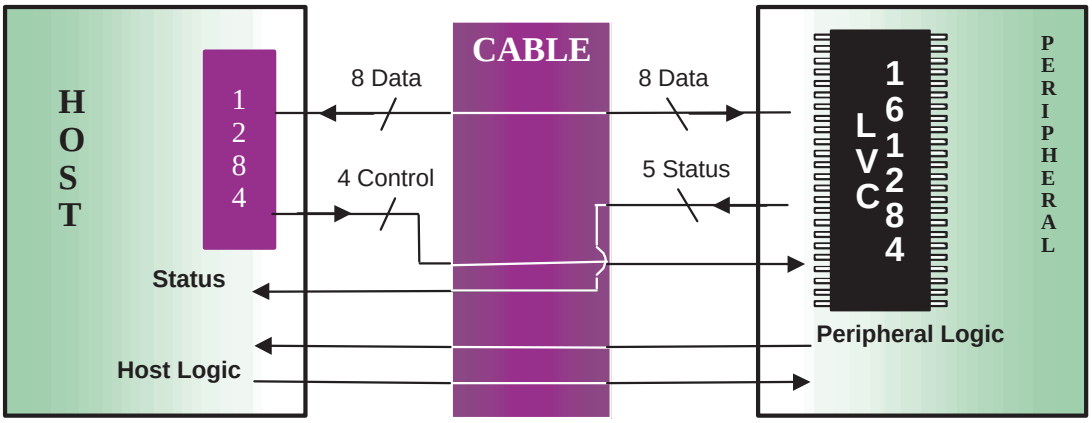


Figure 23. Typical Application Showing a 1284 Interface

Features

- Designed for the IEEE Std 1284-I (Level 1 Type) and IEEE Std 1284-II (Level 2 Type) electrical specifications
- Adds bidirectional capabilities to the existing centronics parallel interface
- Supports 5 modes of data transfer (Centronics; Nibble; Byte; EPP; ECP)
- Advanced operating mode can reach speeds of 16 to 32 Mbps
- New electrical interface, cabling and connector for improved performance and reliability while retaining backward compatibility
- 50 to 100 times faster than the original parallel port (Centronics)

Table 16. Top Device List – IEEE 1284-Compatible Devices

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74ACT1284	TTL	7-bit bus interface with 3-state outputs	20-pin SOP 20-pin SSOP 20-pin TSSOP	Available
SN74LVC161284	LVTTL	19-bit bus interface	48-pin SSOP 48-pin TSSOP	Available
SN74LV161284	LVTTL	19-bit bus interface	48-pin SSOP 49-pin TSSOP	Available

General-Purpose Interface Logic at 5-V and 3.3-V

For a long time TTL-busses have been the standard solution for backplane systems. Different logic families are available to fulfill the requirement for backplane busses. The choice for the appropriate logic strongly depends on physical characteristics of the bus. The main factor is the number of receiving and transmitting modules connected into that bus. The more cards on the backplane, the lower the impedance of the bus due to additional capacitive loading. This arises from the input/output capacitance of the transceivers, the capacitance layer of printed-circuit stub lines and the connectors, resulting in the need for a higher drive capability of the logic device.

Mature 5-V TTL and 5-V CMOS as well as 3.3-V CMOS technologies provide a drive capability of 24 mA and can only handle line impedance down to about 50 Ω. With the introduction of BiCMOS technologies the drive has been enlarged to –32/64mA and with so called incident wave switching drivers (SN74ABT25xxx) it is even possible to drive bus lines with an impedance as low as 25 Ω. The enhanced transceiver logic (ETL) features improved noise margins, while maintaining compatible TTL switching levels and therefore enabling higher speed on the backplane.

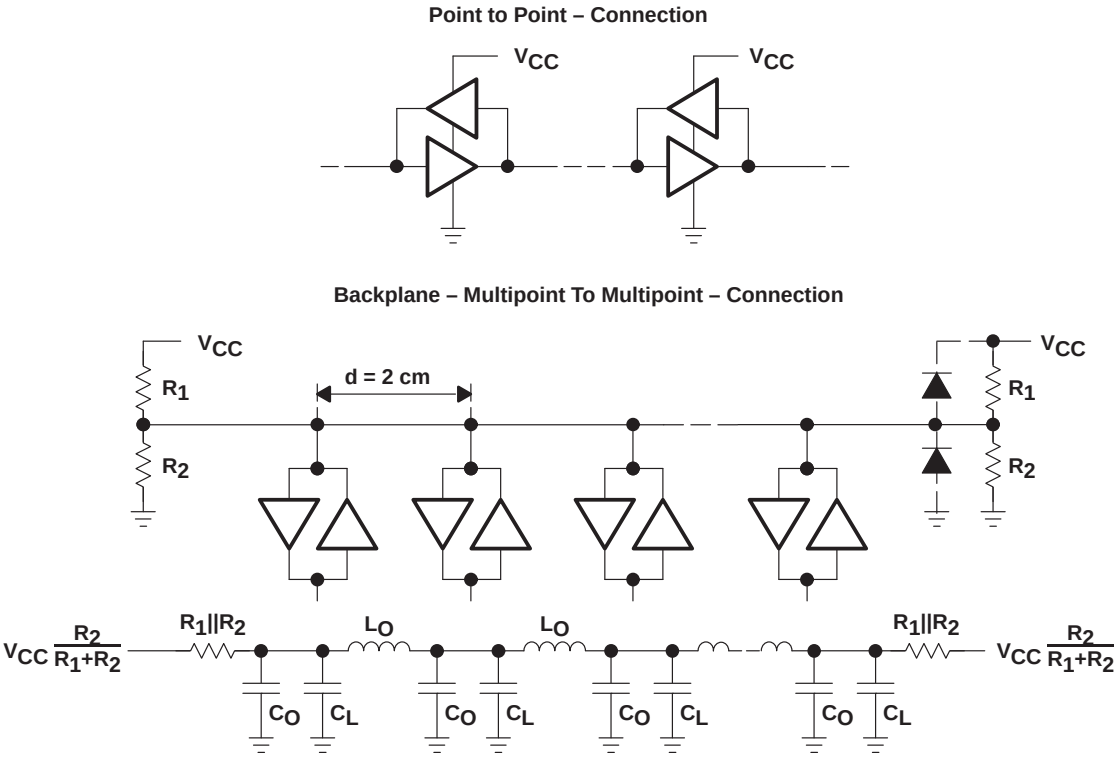


Figure 24. Point-to-Point Connection/Backplane Bus With Replacement Circuit – Showing 1 Bit

Standard logic devices can be used for either point-to-point connections or to realize backplane busses, which consist of many drivers and receivers along the bus, as shown in Figure 24. Both solutions using standard logic devices are usually set up as parallel buses; up to 36 bits can be switched by one logic device. The operational frequency can be chosen within a range from a few MHz up to the clock frequency of about 50 MHz, such that the data-throughput per device is in the range of 1 to 2 Gbps.

Electrical

The electrical specification of LVTTL levels meets the TTL specification. The combination of 5-V TTL with LVTTL is possible without any additional effort. 5-V CMOS levels are not compatible with LVTTL levels:, 5-V tolerance is mandatory for unidirectional and the use of 5-V levelshifters is required for bidirectional data transfer, when combining a 3.3-V system with a 5-V supplied system part. The following table shows the key parameters for 5-V and 3.3-V advanced system logic families. Another important feature is the live insertion capability of a logic family, which enables the user to insert and remove modules during operation. The important parameters are IOFF, Power up/down 3-state, and precharge functionality as shown in Table 17. To get more information about this topic refer to the application report *Live Insertion* (literature code SCZAE07).

Table 17. Selected Characteristics for General-Purpose Logic Families

FAMILY	RECOMMENDED SUPPLY VOLTAGE	DRIVE (mA)	LEVELS	INTERFACING TO (LV) TTL	LIVE INSERTION, REMOVAL HOT INSERTION
AHC	5 V	±8	5 V CMOS	Use level shifter	
AC	5 V	±24	5 V CMOS	Use level shifter	
ABT	5 V	–32/ +64	TTL	Yes	I_{OFF}, PU/D-3-state
ABT25	5 V	–80 (32)/+188 (64)			
ABTE	5 V	–60 (12)/ +90 (12)	ETL	Yes	I_{OFF}, PU/D-3-state and precharge
LVC	3.3 V	±24	LVTTL	Yes	I_{OFF}, (LVCZ: PU/D-3-state)
ALVC	3.3 V	±24	LVTTL	Yes	
LVT	3.3 V	–32/ +64	LVTTL	Yes	I_{OFF}, PU/D-3-state
ALVT	3.3 V	–32/ +64	LVTTL	Yes	I_{OFF}, PU/D-3-state

A maximum bus-length is not specified for backplanes; however, in practice, the bus-length of parallel backplanes does not exceed about 50 cm.

Protocol

Not strictly specified for standard logic families. VME is applicable. ABTE supports VME64

Applicability

The backplanes are not limited to any special domain. They are used in telecom, computer, and industry application, wherever several system parts are connected using a backplane or a memory bus.

SCOPE is a trademark of Texas Instruments.

Features

- 8-,16- and 32-bit devices enable parallel operation on the backplane/memory bus
- Boundary scan devices (JTAG – IEEE 1149.1) available in LVT and ABT enable easy testability during design and production
- Bushold feature eliminates external pullup resistor
- Series damping resistors enable improved signal integrity in point to point busses
- ABT, LVT, ALVT and LVCZ incorporate power up 3-state outputs enabling support hot insertion/removal
- ABTE supports precharge feature enabling support hot insertion/removal
- LVC, ALVC are specified down to 1.8 V, further reducing power consumption

Table 18. Top Feature List of Advanced System Logic by Logic Family

	AHC	AC	ABT	ABTE	(A)LVC	LVT	ALVT
Gates	✓	✓	✓	N/A	✓	N/A	N/A
Flip-flops	✓	✓	✓	N/A	✓	✓	✓
Drivers	✓	✓	✓	✓	✓	✓	✓
Transceivers	✓	✓	✓	✓	✓	✓	✓
UBT™†	N/A	N/A	✓	N/A	✓	✓	✓
Bus hold‡	N/A	N/A	✓	✓	✓	✓	✓
26 Ω Series resistors§	✓	✓	✓	✓	✓	✓	✓
SCOPE™¶	N/A	N/A	✓	N/A	N/A	✓	N/A

† The universal bus transceiver (UBTTM) combines D-type latches and D-type flip-flops for operation in transparent, latched or clocked mode.
‡ Bus hold on data inputs eliminates the need for external pullup resistors.
§ 26 Ω series resistors are included in the output stages, in order to match bus impedance avoiding external resistors
¶ SCOPE™ products are compatible with the IEEE Standard 1149.1-1990 (JTAG) test access port and boundary scan architecture

Figure 25 shows a typical backplane application with several plug-in cards.

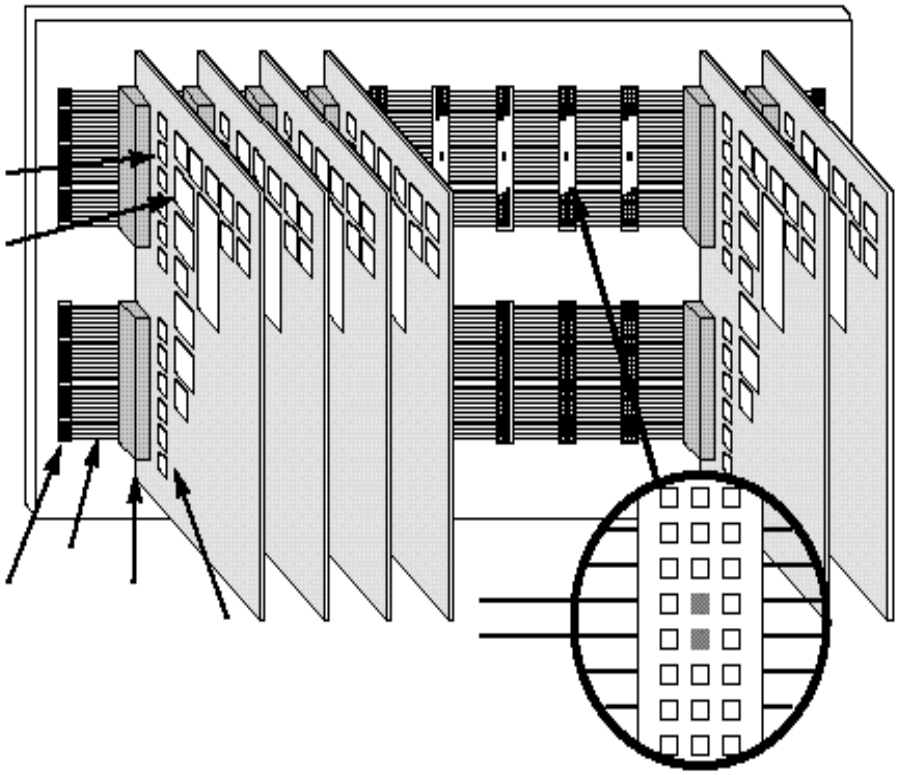


Figure 25. Typical Backplane Application Using Several Plug-In Cards

Backplane Transceiver Logic (SN74FBxxx)

In the past the standard solutions for driving bus lines on backplane systems were TTL or CMOS logic circuits. However, some issues result from the high voltage swing of 3.3 V up to 5 V: Correct termination for all load conditions is not possible and large drive capabilities are necessary to enable incident wave switching.

A bus system with reduced voltage swing solves a lot of problems. The BTL bus realizes a bus in open collector mode, as shown Figure 26. In this case, the falling edge is actively generated from the driver. Only a low impedance driver can switch the bus with the incident wave.

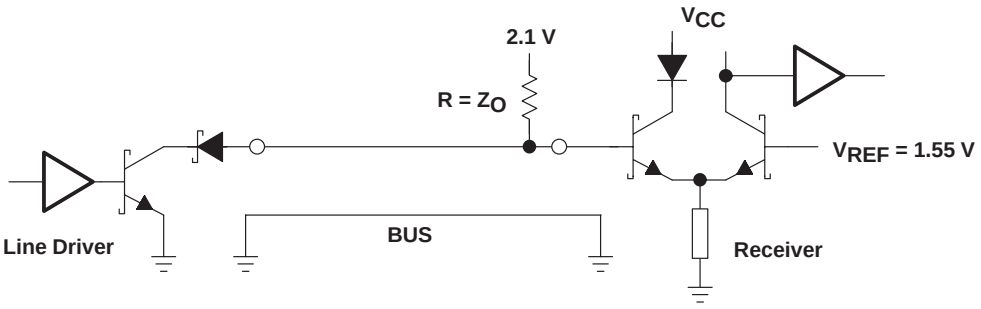


Figure 26. Principle Setup of an Open Collector Bus System Using BTL Devices

Electrical

The physical layer of the Futurebus is called backplane transceiver logic (BTL) and works with a voltage swing of 1.1 V only using an open collector bus system. The saturation voltage of the pulldown transistor and the forward voltage of the serially connected diode generates the output low level voltage of 1 V. The high level of 2.1 V comes from the termination resistor connected to the termination voltage of 2.1 V. The value of the termination resistor is equal to the impedance of the bus-line and therefore the bus-line is terminated correctly. For safe detection of the logic levels, the inputs are designed with differential amplifiers and a threshold at 1.55 V, exactly in the middle of the voltage swing.

To reduce ICC current spikes, the fall-time is defined to be 2 ns or slower. The rise time is not generated by active electronics, but by the pullup resistor.

Protocol

Futurebus plus logical layer specification, according to the IEEE896.2 specification, describes the node management, live insertion, and profiles. However the physical layer may also be used stand-alone without the logical layer.

Applicability

The target area for BTL devices is the telecom sector, where especially the live insertion capability is mandatory.

Features

- Reduced voltage swing: V_L = 1 V; V_H = 2.1 V generates low switching noise 10 Ω or 20 Ω || 20-Ω line impedance
- Correct line termination by a pullup resistor at the line end avoids line reflections
- Decoupling diode reduces output capacitance to < 5 pF, increases line impedance
- Maximum output edge rate 2 ns, trapezoidal wave-form reduces system noise
- Supports live insertion/withdrawal

Table 19. Top Device List – Backplane Transceiver Logic

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74FB2033A	TTL/BTL	8-Bit TTL/BTL registered transceivers	52-pin PQFP	Available
SN74FB1651	TTL/BTL	17-Bit TTL/BTL universal storage transceivers with buffered clock times	100-pin SQFP	Available
SN74FB2031	TTL/BTL	9-Bit TTL/BTL address/data transceivers	52-pin PQFP	Available
SN74FB1653	LVTTL/BTL	17-Bit LVTTL/BTL universal storage transceivers with buffered clock lines	100-pin SQFP	Available
SN74FB2041A	TTL/BTL	7-Bit TTL/BTL transceivers	52-pin PQFP	Available
SN74FB2040	TTL/BTL	8-Bit TTL/BTL transceivers	52-pin PQFP	Available

Gunning Transceiver Logic (SN74GTLxxx) – SN74GTL1655

The basic concept of a GTL bus is similar to a BTL system and is shown in Figure 27.

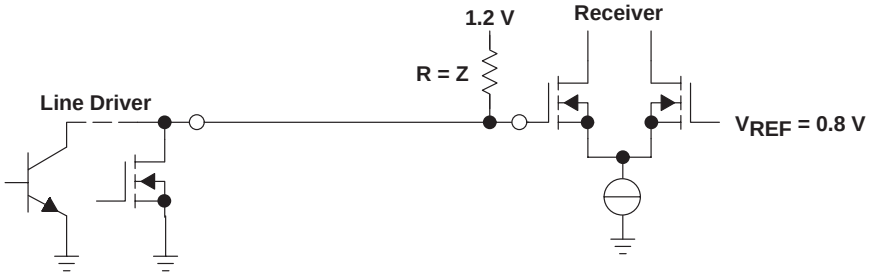


Figure 27. Principle Setup of an Open Collector Bus System Using GTL Devices

Because of the missing diode in the open collector/drain outputs (compared to the BTL–solution) the low level is 0.4 V. With a chosen high level of 1.2 V the voltage swing is reduced to 0.8 V only. Again the threshold is in the middle of the voltage swing at 0.8 V.

With a drive capability of GTL outputs up to about 40 mA, the GTL devices are able to drive a termination resistor of 0.8 V/40 mA = 20 Ω. If the bus line is terminated correctly, the lowest impedance that can be driven by a GTL driver in the middle of a bus is 40 Ω (effectively the driver sees: 40 Ω || 40 Ω = 20 Ω). As a result of the 0.8 V swing and the 40 mA IOL, the maximum power dissipation of one output is 16 mW. It is thus possible to integrate these low power drivers into ASICs.

Specialties of the GTL Device SN74GTL1655

With the SN74GTL1655 the benefits of the BTL family and GTL family are combined within one device. The drive capability of the SN74GTL1655 outputs now provides up to 100 mA, enabling the outputs to drive a termination resistor of 11 Ω.

With the GTL1655 even heavily loaded backplane busses can be served. For those busses the line impedance can decrease down to 22 Ω.

All the features for live insertion and withdrawal have also been included in the GTL1655. The SN74GTL1655 further includes a selectable edge rate control circuit (ERC) for variable rise and fall rates so that the designers can fine tune their circuits for maximum data throughput as system loading dynamically changes. The edge rate control minimizes bus-settling time.

Electrical

The gunning transceiver logic (GTL) devices support two different logic level specifications: GTL (according EIA/JEDEC Standard EIA/JESD8-3) and the GTL + levels. The bus system is — similar to the BTL bus — realized as open collector bus. There is no diode included in the open collector/drain output stage of the GTL-devices, such that the output low level could be reduced down to 0.4V (GTL+: 0.55). With a chosen high level of 1.2 V for GTL (GTL+: 1.5 V) the voltage swing is reduced to 0.8V (0.95 V) only. The threshold is in the middle of the voltage swing at 0.8 V (GTL+: 1 V).

GTL+ is becoming more and more a standard in the industry due to the enlarged noise margin of GTL+ levels. For example GTL+ levels are being used on the Intel Pentium Pro (P6) processor to address this noise margin concern. Using GTL+ levels instead of GTL, the margin is increased about 16 %.

Protocol

Not specified.

Applicability

GTL was originally designed for a small bus on a board, for example, between a processor and its memory modules. Because the target application for GTL is not a backplane bus, but a bus on a board, no requirements for live insertion/withdrawal have been included in the specification.

With reduced output levels and state-of-the-art designs, the consequences are reduction of power consumption, higher speeds, and improved signal integrity compared to the BTL-bus, such that GTL+ backplane optimized – drivers are a premium solution for heavily loaded bus systems. Live insertion capabilities and an increased drive for low impedance backplanes are met with the GTL1655 device.

Features

- Differential amplifier guarantees stable threshold voltage of the receiver
- Low voltage swing generates low switching noise
  - GTL: V_L = 0.4 V; V_H = 1.2 V
  - GTL+: V_L = 0.55 V; V_H = 1.5 V
- High drive capable option available, enabling incident wave switching as low as 10 Ω or 20 Ω || 20 Ω line impedance
  - GTL/GTL+: Low drive capability, I_{olmax} = 40/50 mA
  - GTL1655: High drive capability, I_{olmax} = 100 mA
- Correct line termination using a pullup resistor at the line end avoids line reflections
- Edge rate control output circuit of GTL1655 enables variable output slew-rate depending on load condition for maximum data throughput.

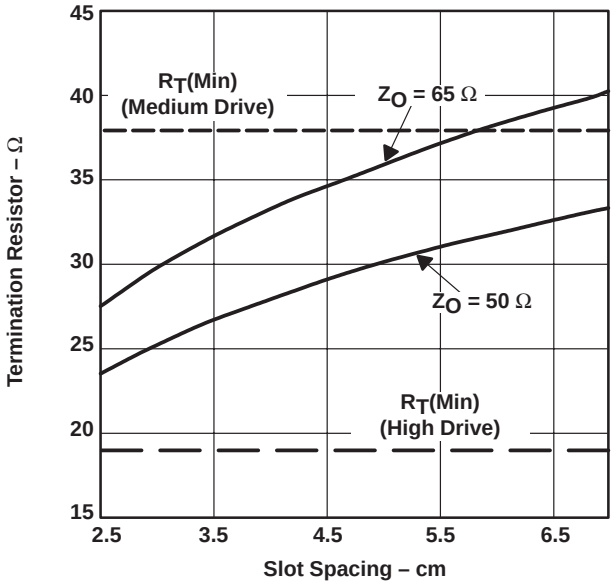
Table 20. Top Device List GTL

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTL16612	LVTTL/GTL	18-Bit LVTTL/GTL+ universal bus transceivers, like 16601 function	56-pin SSOP 56-pin TSSOP	Available
SN74GTL1655	LVTTL/GTL	17-Bit LVTTL/GTL+ universal bus transceivers with live insertion, like 16501 function	64-pin TSSOP	Available
SN74GTL16616	LVTTL/GTL	16-Bit LVTTL/GTL+ universal bus transceivers with buffered clock outputs, like 16601 function	56-pin TSSOP 56-pin SSOP	Available
SN74GTL16622A	LVTTL/GTL	18-Bit LVTTL/GTL+ bus transceivers, like 16601 function w/o LE and two CE	64-pin TSSOP	Available
SN74GTL16923	LVTTL/GTL	18-Bit LVTTL/GTL+ bus transceivers, like 16601 function w/o LE and two OE	64-pin TSSOP	Available

Gunning Transceiver Logic Plus (SN74GTLPxxx)

GTLP devices are high-speed transceivers (LVTTL/card and GTLP/backplane) that operate like the GTL family except for two major differences: they have been optimized for the distributed loads found in multi-slot backplanes and they support live insertion with internal precharge circuitry. The GTLP reduced output swing (<1 V) and reduced input threshold levels allow higher backplane clock frequencies increasing the bandwidth for manufacturers developing next generation telecommunication and data communication solutions. GTLP devices are backward compatible with commonly used parallel backplane technologies such as ABT, FCT, LVT, ALVT, and FB+ and provided an alternative to more complex serial technologies.

GTLP offers two different drives, 50 and 100 mA recommend I_{OL} at 0.55 V, to allow the designer flexibility in matching the device to backplane length, slot spacing and termination resistor. The medium drive device can drive lines in point-to-point configurations down to 19 Ω. The lowest termination resistor that can be driven by the driver in the middle of a bus is 38 Ω (effectively the driver's load is 38 Ω || 38 Ω = 19 Ω). The high drive devices can drive loads of 9.5 Ω (0.95 V/100 mA). So the minimum termination resistor for bus configuration will be 19 Ω. It is important to pick a termination resistor that matches the backplane impedance for best signal integrity but is within the capacity of the driver. Impedance is a function of natural trace impedance (Z_O), stub length, connector impedance, device impedance, and card spacing. Closer spacing reduces the effective impedance, which requires a smaller termination resistor as shown in Figure 28.



NOTE: Assumption: 12 pF/card

Figure 28. R_T Versus Slot Spacing With GTLP Medium and High Drive Devices

Electrical

Optimized for the GTLP signal level specifications, also operates at GTL (according JEDEC Standard JESD8-3) or GTL+ signal levels. The bus system, identical to the GTL bus, is realized as an open drain bus. The GTLP voltage swing is from 1.5 V to 0.55 V with ±50 mV around the V_{REF} threshold of 1 V.

Protocol

Not specified.

Applicability

GTLP is used where the major concerns are higher data throughput, live insertion capability or lower power consumption in parallel backplane architectures. GTLP offers up to four times the performance of TTL devices in backplane upgrade applications.

Features

- 3.3-V operation with 5-V-tolerant LVTTL inputs/outputs which allow the devices to act as 5-V TTL to GTLP as well as 3.3-V LVTTL to GTLP translators
- Significantly improved output edge control (OEC) circuitry on the rising and falling edge of the GTLP outputs reduces line reflections, electromagnetic interference (EMI) and improves overall signal integrity allowing clock frequencies in excess of 80 MHz.
- Fully supports live insertion with I_{off}, PU3S and BIAS V_{CC} circuitry
- Edge rate control (ERC) circuitry on high drive devices allows fast or slow edge rates.
- CMOS construction for 1/3 the static power consumption of BiCMOS logic devices
- A-port (LVTTL side) balanced drive of $\pm$24 mA with optional bus-hold circuitry

Table 21. Top Device List GTLP

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTLPH306	LVTTL/GTLP	8-bit LVTTL/GTLP medium drive bus transceivers	24-pin SOIC 24-pin TSSOP 24-pin TVSOP	DUD sample
SN74GTLP817	LVTTL/GTLP	GTLP/LVTTL medium drive with ERC 1:6 fanout driver	24-pin SOIC 24-pin TSSOP 24-pin TVSOP	Product preview
SN74GTLPH16912	LVTTL/GTLP	18-bit LVTTL/GTLP medium drive universal bus transceivers	56-pin SSOP 56-pin TSSOP 56-pin TVSOP	Product preview
SN74GTLPH16945	LVTTL/GTLP	16-bit LVTTL/GTLP medium drive bus transceivers	48-pin SSOP 48-pin TSSOP 48-pin TVSOP	Product preview
SN74GTLPH32912	LVTTL/GTLP	36-bit LVTTL/GTLP medium drive universal bus transceivers	114-ball LFBGA	Product preview
SN74GTLPH32945	LVTTL/GTLP	32-bit LVTTL/GTLP medium drive universal bus transceivers	96-ball LFBGA	Product preview
SN74GTLP1394	LVTTL/GTLP	2-bit LVTTL/GTLP high drive bus transceivers with ERC	16-pin SOIC 16-pin TSSOP 16-pin TVSOP	DUD sample
SN74GTLPH1612	LVTTL/GTLP	18-bit LVTTL/GTLP high drive universal bus transceivers with ERC	64-pin TSSOP	Product preview
SN74GTLPH1645	LVTTL/GTLP	16-bit LVTTL/GTLP high drive bus transceivers with ERC	56-pin SSOP 56-pin TSSOP 56-pin TVSOP	DUD sample
SN74GTLPH1655	LVTTL/GTLP	16-bit LVTTL/GTLP high drive universal bus transceivers with ERC	64-pin TSSOP	DUD sample
SN74GTLPH3245	LVTTL/GTLP	32-bit LVTTL/GTLP high drive bus transceivers with ERC	114-pin LFBGA	Product preview
SN74GTLPH16612	LVTTL/GTLP	18-bit LVTTL/GTLP medium drive universal bus transceivers	56-pin SSOP 56-pin TSSOP	Available

Stub Series Terminated Logic (SN74SSTLxxx)

Designers are constantly trying to get the most out of their designs in the most cost-effective means. As faster versions of a particular CPU become available, the designer often will try to improve the throughput of an existing design simply by increasing the CPU clock frequency.

These issues resulted in JEDEC defining two SSTL switching standards (SSTL_3, EIA/ JESD8-8, SSTL_2, EIA/ JESD8-8). Both standards specify a particular termination scheme with appropriate values for the resistors and capacitors.

The stub series-terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The primary application for SSTL devices is to interface with SDRAMs.

Two resistors in parallel are used to establish a voltage level such that differential voltage swings can be utilized and two different resistor value configurations can be acceptable.

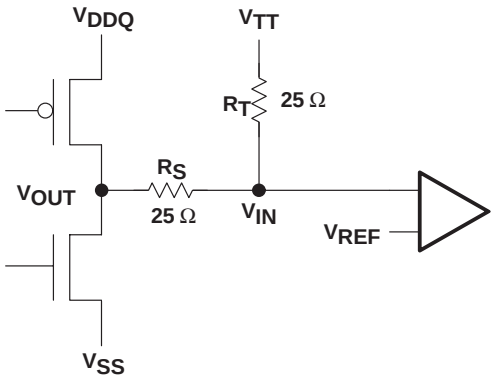


Figure 29. Typical Output Buffer Environment, Class II of SSTL Standard

Class I specifies an acceptable value of 50 Ω for the termination resistor R_T, and Class II specifies an acceptable value of 25 Ω. Figure 29 shows the typical dc environment for the output buffer (Class II), in this case an additional series resistor R_S is specified at 25 Ω. In order to meet the 400 mV minimum requirement for VIN, a minimum of 8 mA must be driven into R_T, if R_T equals 50 Ω (Class I); or 16 mA if RT equals 25 Ω (Class II). The standard states that for each value of R_T, a capacitive load equal to 10 pF or 30 pF can be used. The SSTL16837A supports both SSTL and LVTTL switching levels. Although the data sheet provides specifications where SSTL levels are used for the input and output levels, the device can operate under any combination of SSTL/LVTTL levels for the inputs and the outputs. When SSTL levels are applied to the device, it functions approximately 2 ns faster than using LVTTL levels.

Electrical

The stub series-terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The input high and low voltage levels (V_{IH} and V_{IL}) are V_{REF} +200 mV and V_{REF} –200 mV, resulting in a worst case noise margin of 25%. This seems to be a relatively small noise margin, but since it is a terminated bus, the actual noise source would have to be a fairly high current to produce 400 mV across the relatively low-impedance termination.

All totem-pole outputs of the SSTL compatible devices have a dedicated V_{DDQ} supply that (as stated in the SSTL_3 and SSTL_2 JEDEC standards) can be lower than or equal to V_{DD}, but never greater than V_{DD}. This feature allows for the internal circuitry supply voltage to be raised to 3.6 V for maximum speed performance, while lowering V_{DDQ} to prevent the device from dissipating large amounts of power in the output stage.

Irrespective of the input and output switching levels however, the characteristic high-level and low-level output drive current of 20 mA is maintained.

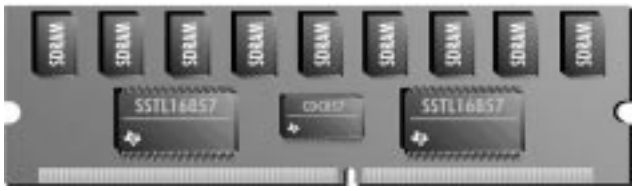
Protocol

Not specified.

Applicability

Figure 30 shows a complete DDR SDRAM (SDRAM II) memory interfacing solution offered from Texas Instruments. Using a specially designed register, low-voltage bus switches, and a differential clock, DDR SDRAM modules can achieve double the memory data rate by allowing the SDRAMs to operate at twice their system frequency using the rising and the falling edge of the system clock.

The 14-bit registered buffer SSTL16857 is designed for 2.3-V to 3.6-V V_{CC} operation and differential data input and output levels. It buffers DDR SDRAM address and control signals. The CDC857 differential clock completes the TI solution for 184-pin DDR SDRAM modules. Optionally, the SSTL_2 optimized CBTLV3857 provides bus isolation in the DDR SDRAM DIMM application and reduces the capacitive loading on the data lines.



Front View

Back View

Figure 30. DDR SDRAM Memory Interfacing Solution Using the SN74SSTL16857

Features

- Maximum frequency of 200 MHz enables fast DDR SDRAM memory busses
- Supports both SSTL and LVTLL switching levels, which enables any combination of SSTL and LVTTL levels for inputs and outputs

- SSTL and LVTTL levels for inputs and outputs
- Outputs have dedicated V_{DDQ}, which can be lower or equal to V_{DD}. This enables the internal circuitry supply voltage to be raised to 3.6 V for maximum speed, while lowering V_{DDQ} to prevent the device from large power dissipation in the output stage.

Table 22. Top Device List for Stub Series Termination Logic

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74SSTL16837A	SSTL_3	20-Bit SSTL_3 interface universal bus driver with 3-state outputs	64-pin TSSOP	Available
SN74SSTL16847	SSTL_3	20-Bit SSTL_3 interface buffer with 3-state outputs	64-pin TSSOP	Available
SN74SSTL16857	SSTL_2	14-Bit SSTL_2 registered buffer	48-pin TSSOP	Planned
SN74SSTL32867	SSTL_2	26-Bit registered buffer with SSTL_2 differential inputs and LVCMOS outputs	96-ball LFGBA	Planned
SN74SSTL32877	SSTL_2	26-Bit registered buffer with SSTL_2 differential inputs and outputs	96-ball LFGBA	Planned

Summary

This *Comparing Bus Solutions* application report shows that Texas Instruments provides a vast portfolio of data transmission products covering most of the commonly used communication standards. The offering ranges from typical backplane logic families like ABT, LVT and GTLP to more advanced serial transmission families like LVDS and IEEE1394, while still providing solutions for the mature TIA/EIA (nee RS) standards such as 232 and 485.

By referring to this application report, choosing the correct standard and therefore the appropriate family has been made easier. Simply by selecting the type of transmission, that is, serial or parallel, the distance and the data rate, a designer can very quickly find what he needs and has an introduction to the family contained in the report, with internet pages waiting to be browsed for additional information.

Altogether, this shows that Texas Instruments is committed to maintaining a leadership position in the field of data transmission, and TI will continue to increase the range of advanced products available to engineers.

References

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3. ISO/IEC 9316, Information Technology, Small Computer System Interface-2
4. EIA/TIA-232-E, ITU-T V.28
5. TIA/EIA-644, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
6. EIA/JESD8-A, Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits
7. EIA/JESD8-3, Gunning Transceiver Logic (GTL), Low-Level, High-Speed interface Standard for Digital Integrated Circuits
8. IEEE1394-1995, High Performance Serial Bus
9. IEEE P896.1, Futurebus+ Logic Layer Specifications
10. IEEE P896.2, Futurebus+ Physical Layer and Profile Specifications
11. EIA/JESD8-8, Stub Series Terminated Logic for 3.3 V (SSTL_3)
12. EIA/JESD8-9, Stub Series Terminated Logic for 2.5 V (SSTL_2)
13. IEEE802.3z Gigabit Task Force
14. GMII Gigabit Media Independent Interface
15. USB Universal Serial Bus Specification Revision 1.1 (Compaq, Intel, Microsoft, NEC)

Glossary

ABT	Advanced BiCMOS technology, 5-V logic family with TTL-compatible input and output specification
ABTE	Enhanced transceiver logic. 5-V logic with reduced noise margins to achieve higher speeds on the backplane, TTL-compatible
Arbitration	The process by which nodes compete for ownership of the bus. The cable environment uses a hierarchical point-to-point algorithm, while the backplane environment uses the bit-serial process of transmitting an arbitration sequence. At the completion of an arbitration contest only one node will be able to transmit a data packet.
BTL	Backplane transceiver logic. Typical applications are parallel backplanes
BPS	Bits per second
DDR SDRAM	Double data rate synchronous dynamic random access memory
Downstream	The direction of data flow from the host or away from the host. A downstream port is the port on a hub electrically farthest from the host that generates downstream data traffic from the hub. Downstream ports receive upstream data traffic.
EMI	Electromagnetic interference
Endpoint	An endpoint that is capable of consuming an isochronous data stream that is sent by the host.
GTL	Gunning transceiver logic. GTL+ and GTLP are derivatives of GTL that operate at enhanced noise margin signal levels (V_{TT} = 1.5 V, V_{REF} = 1 V and V_{OL} = 0.55 V). GTLP is normally associated with optimized edge rate devices that allow high frequency operation in heavily loaded backplane applications.
Hub	A USB device that provides additional connections to the USB. Typical applications are parallel backplanes
HVD	High voltage differential
Isochronous	The term isochronous indicates the essential characteristic of a time-scale or a signal such that the time intervals between consecutive significant instances either have the same duration or multiples of the shortest duration.
Life Insertion/Removal	The ability to attach and remove devices while the system is in operation
Link layer	The layer, in a stack of three protocol layers defined for the serial bus, which provides the service to the transaction layer of one-way data transfer with confirmation of reception. The link layer also provides addressing, data checking, and data framing. The link layer also provides an isochronous data transfer service directly to the application.

LVD	Low voltage differential
LVDM	Low voltage differential signaling for multipoint applications
LVDS	Low voltage differential signaling
LVTTL	Low voltage transistor-transistor-logic
Mode	An addressable device attached to the serial bus with at least the minimum set of control registers. Changing the control registers on one node does not affect the state of control registers on another node.
NRZI	Non return to zero invert. A method of encoding serial data in which ones and zeroes are represented by opposite and alternating high and low voltages where there is no return to zero (reference) voltage between encoded bits. Eliminates the need for clock pulses.
Packet (1394)	A serial stream of clocked data bits. A packet is normally the PDU for the link layer, although the cable physical layer can also generate and receive special short packets for management purposes.
Packet (USB)	A bundle of data organized in a group for transmission. Packets typically contain three elements: control information (e.g., source, destination, and length), the data to be transferred, and error detection and correction bits.
Physical layer	The layer, in a stack of three protocol layers defined for the serial bus, which translates the logical symbols used by the link layer into electrical signals on the different serial bus media. The physical layer guarantees that only one node at a time is sending data and defines the mechanical interface for the serial bus. There is a different physical layer for the backplane and for the cable environment.
Pipe	A logical abstraction representing the association between an endpoint on a device and software on the host. A pipe has several attributes; for example, a pipe may transfer data as streams (stream pipe) or messages (message pipe).
PLL	Phased lock loop: The PLL circuits is a feedback circuit. The purpose of this circuit is to minimize phase error between the input signal and the output signal of the PLL. In the locked state the PLL regulates continuously the phase between the f_{in} and f_{out}, such a defined phase difference between both frequencies is maintained.
Port	A physical layer entity in a node that connects to either a cable or backplane and provides one end of a physical connection with another node.
RS	Recommended standard
SCSI	Small computer systems interface
SSTL	Series stub termination logic
Stubs	Short traces, branching from the backplane. Often found on memory modules.

Termination resistor	The termination resistor is used at the end of a line in order to avoid reflections of the transmitted signal. If the termination resistor is chosen equally to the line impedance the line is optimally terminated.
Transaction	The delivery of service to an endpoint; consists of a token packet, optional data packet, and optional handshake packet. Specific packets are allowed/required based on the transaction type.
Transfer	One of the four USB transfer types. Isochronous transfers are used when working with isochronous data. Isochronous transfers provide periodic, continuous communication between host and device.
Quadlet	Four bytes of data.
USB	Universal serial bus
Upstream	The direction of data flow towards the host. An upstream port is the port on a device electrically closest to the host that generates upstream data traffic from the hub. Upstream ports receive downstream data traffic.

TI Contact Numbers

INTERNET		***Asia***	
TI Semiconductor Home Page		Phone	
www.ti.com/sc		International	+886–2–23786800
TI Distributors		Domestic	
www.ti.com/sc/docs/distmenu.htm		***Australia***	1–800–881–011
PRODUCT INFORMATION CENTERS		TI Number	–800–800–1450
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Phone	+1(972) 644–5580	TI Number	–800–800–1450
Fax	+1(972) 480–7800	Hong Kong	800–96–1111
Email	sc–infomaster@ti.com	TI Number	–800–800–1450
Europe, Middle East, and Africa		***India***	000–117
Phone		TI Number	–800–800–1450
Deutsch	+49–(0) 8161 80 3311	***Indonesia***	001–801–10
English	+44–(0) 1604 66 3399	TI Number	–800–800–1450
Español	+34–(0) 90 23 54 0 28	***Korea***	080–551–2804
Francais	+33–(0) 1–30 70 11 64	***Malaysia***	1–800–800–011
Italiano	+33–(0) 1–30 70 11 67	TI Number	–800–800–1450
Nordic Countries		***New Zealand***	000–911
Fax	+44–(0) 1604 66 33 34	TI Number	–800–800–1450
Email	epic@ti.com	***Philippines***	105–11
Japan		TI Number	–800–800–1450
Phone		***Singapore***	800–0111–111
International	+81–3–3457–0972	TI Number	–800–800–1450
Domestic	0120–81–0026	***Taiwan***	080–006800
Fax		***Thailand***	0019–991–1111
International	+81–3–3457–1259	TI Number	–800–800–1450
Domestic	0120–81–0026	Fax	886–2–2378–6808
Email	pic–japan@ti.com	Email	tiasia@ti.com

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