High-Side SmartFETs with Analog Current Sense

AND9733/D

INTRODUCTION AND SCOPE

This application note describes the structure and design philosophy of **onsemi** High Side SmartFETs, and serves as a guide to understand the operation of the device in specific applications. The scope of this document is limited to SmartFETs with analog current sense output. The following section covers the application details and behavior of specific application loads. This is followed by Section Power FET and Protection that provides details on the physical structure of the power element− the vertical power FET and different technologies employed to realize the power FET. This section also includes the protection features incorporated within the device that enable it to protect itself in case a system failure condition exists. Section Application interface and control describes the application interface to the SmartFET and provides recommendations for the peripheral circuit for the desired operation. The switching characteristics of the device while driving typical automotive loads are explained in Section Switching Characteristics.

The subsequent section elaborates the operation of the analog current sense and fault reporting through the diagnostic output multiplexed with the current sense output. Since the fault flagging conditions could be different for different devices in the family, it is always recommended to refer to individual product datasheets for the specific diagnostic truth table. This document encompasses the typically observed fault conditions and describes the behavior of device and expected the current sense operation for those faults. Finally, the last section provides an understanding of the thermal response of the device and also outlines the interpretation of thermal data and curves published in the product datasheets. This would help in designing the correct application heat sinking and PCB layout to obtain the optimal thermal performance from the device.

The document also provides specific examples and numerical calculations while explaining certain concepts. It should be noted that unless otherwise mentioned, the values mentioned in these examples should be considered only typical and not defining any bounds on the performance of the device. For all maximum ratings, the respective product datasheets should be referred. In addition, any layouts or circuit blocks depicted in this document are exemplary and do not necessarily represent an actual die or a real circuit schematic drawing of a specific device. Lastly, the waveforms have been idealized to explain the behavior of device inputs/outputs under certain scenarios.

APPLICATION SYSTEM OVERVIEW

The design flow for any device initiates with a holistic understanding of the target application environment followed by specification creation around the required performance in application. The close interaction with application and an intricate dependence (of a device's performance) on external conditions necessitate adopting a system level approach for a design guide. Therefore, before discussing the device specifics, it is imperative to understand the application environment, behavior of typical loads and their interaction with the high side switches.

Smart High Side Switches − Motivation

The "end requirement" from a high side SmartFET is to switch loads, and there are different alternatives, available in market, towards that end. Relays, for instance, have been used for long in the industry to switch various automotive loads, especially those requiring high current activation. With a continual reduction in the weight and size of automotive components and assemblies, there has been an evident transition from relays to semiconductor switches that take up less area and also offer improved noise immunity and lower electromagnetic interference as compared to relays.

A p−n junction diode is an easy to use semiconductor switch that solves the basic requirement of switching. However, the power dissipations and high conduction losses do not render them as a viable alternative in the modern automotive environment with aggressive target specs on improving efficiency and cutting down system losses. Further, the bipolar nature of the conduction element involves minority carrier injection and extraction during switching that limits the speed in application. Devices like SCR's (Silicon controlled rectifiers) and triacs also face similar challenges. Bipolar transistors have high output current drive capabilities and lower conduction losses (than diodes) but require an input current drive that makes them undesirable as a switching element. They are widely used in semiconductor industry, however, for bandgap generation and voltage regulation purposes. Applications requiring high voltage breakdown with a reasonably high output current drive, such as fuel ignition, typically employ IGBTs as the switching element. Since the output stage in an IGBT is bipolar, the minority carrier extraction, as for any p−n junction, limits the turn−on/turn−off rates. With a focus on all the performance metrics discussed above, a FET is the most likely and widely used candidate for switching automotive loads. Ease of input drive, high input

December, 2021 − Rev. 1
Publication Order Number:
AND9733/D

impedance, fast switching and a wide SOA (Safe Operating Area) help in achieving the optimal switching performance.

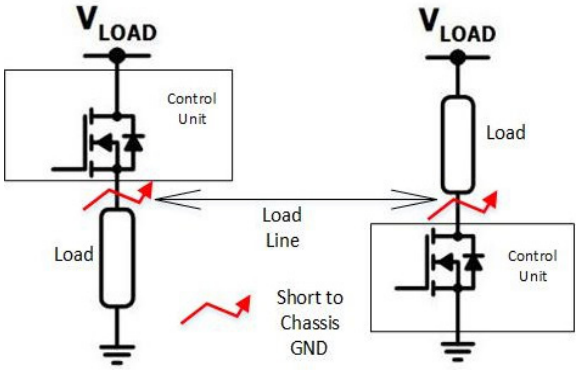

Figure 1. High−Side Switch vs Low−Side Switch in an Application

Figure 1 depicts two of many topologies used for switching loads in an application. With a high side switch, the load is always connected to the ground and the connection to the supply is switched; with a low side switch, the load is always connected to the power supply and the connection to GND is switched. The switch is typically housed inside a control unit or, ECU. The load line is the cable length that connects the load to the pin connector on the ECU. Depending on the load type and its location in the vehicle, this load line could be fairly long, thereby, increasing the likelihood of a short to chassis ground which could be a severely stressful condition for the load in a low−side configuration. This makes the high side switches a preferred choice for load switching. In addition, in cases where a parasitic impedance path to GND exists in the system (as would be described in later sections that temperature and humidity can create leakage resistances over time), the leakage levels are higher in a low side configuration where power supply is always connected to the load. With the advancement in charge pump design and technology, it is relatively convenient to integrate charge pump with the power element, enabling N−channel FETs to be used in high side configuration in a small chip size.

Some applications also use an H−Bridge switching configuration to drive bi−directional loads− for example, a door lock/unlock motor. An H−bridge utilizes two pairs of high side and low side switches as shown below:

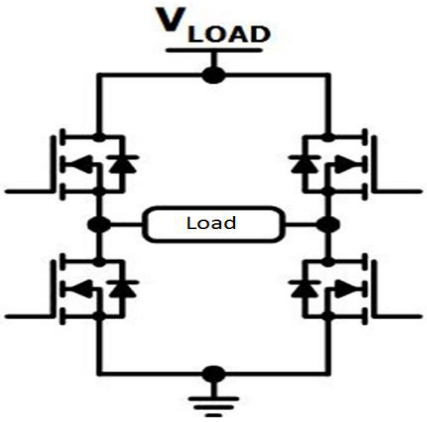

Figure 2. H−Bridge Switching Configuration

With the increasing complexity in application (to render more features available to the user), the probability of a system failure condition also increases. This requires the switch to protect itself in case of operation outside the intended regime, most likely due to a system failure condition (such as output short circuit to GND) existing. From a cost point of view, adding smarts to a switch eliminates the cost of replacement (in certain safety critical applications, the whole module needs to be replaced in case a device fails) and reduces the system cost over an extended period. While adding control and logic features to the power FET, due care has to be exercised in the device design stage to ensure the required module reliability.

Hide Side SmartFET Solutions

onsemi High Side SmartFETs are offered in monolithic or dual die solutions. Figure 3 highlights, in dashed rectangles, the two sections of a SmartFET− the control circuit (consisting both analog, digital controls and the charge pump) and a power section (consisting the power DMOS and sense elements for temperature and current sensing). In a monolithic solution, as the name suggests, both these sections are integrated on the same substrate while in a dual die solution, these two sections are realized on two different substrates and connected with inter−die bonds. The relative orientation and integration of the two dies depends on required package dimensions and device's long term reliability. Section Monolithic vs Dual Die Technology provides a detailed description of these solutions along with their benefits and drawbacks.

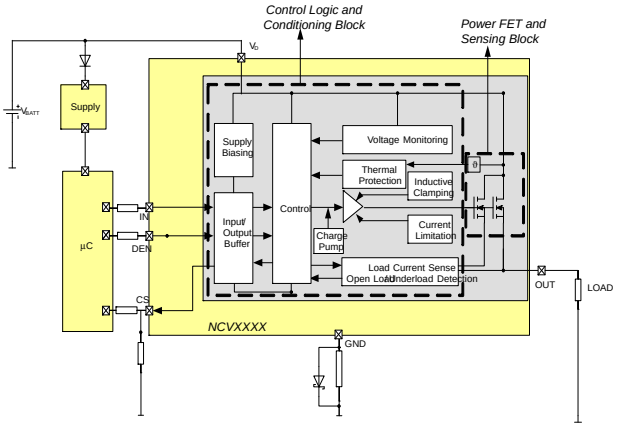

Figure 3. Block Diagram Highlighting the Power FET And The Control Section

Within the power FET section, the technology can vary between a planar and a trench gate stack for the vertical DMOS (Refer Section Planar vs Trench FET). The choice of solution for a particular device is primarily governed by the normalized on state resistance targeted in a given package (a trench FET, in general, will have a lower on−state resistance than a planar FET for a given silicon area) while considering other factors including, but not limited to, required output current drive and sense capability, and the thermal response of the die (Refer Section Understanding the Thermal Network for details on the thermal behavior). In addition, manufacturability and process costs are also considered before determining the technology for a given device. **onsemi** High Side SmartFETs are designed considering that the performance parameters, protection and diagnostic feature set, and the desired operation in application are not affected by the underlying technology.

It should be highlighted here that some high−side SmartFETs are equipped with one−time programmable trims (OTP) in the form of an array of fuses that are programmed at the end of production line. The “trimming” process starts by evaluating the performance of “untrimmed” devices first. Based on any deviation from the desired spec, these trims (or fuses), then serve as inputs to the control logic, which subsequently alters the performance on silicon to closely align it with the spec. Implementing such a sequence allows for an improved tolerance on timing and protection parameters such as the short circuit current limit, switching times etc.; reduces device−to−device variability; and provides an enhanced design flexibility. The trim structures realized on the die undergo the required reliability stress and are ensured to adhere to lifetime operation standards. The devices with trim capability can only be programmed at the end of the production line and are not offered to be programmed in field by the customers for safety concerns. Effect of trims on the product performance will be discussed individually for specific blocks and parameters through this document.

Application Environment and Loads

The automotive application environment is vastly different and typically more aggressive in requirements than other applications like industrial, consumer etc. Standards including AEC−Q100 require automotive switches to adhere to a minimum standard of quality, reliability and robustness under extremes of ambient variations (temperature, pressure humidity etc.).

Consider, for example, a scenario of switching a bulb load. As will be described later in this section, incandescent lamps require an inrush current at turn−on, which is higher than the nominal drive current. The bulb load in this example is an H4 type headlamp rated for a nominal power of 55 W at 12.8 V. The inrush current required at an ambient temperature of ~300 K (27 °C) is ~75 Amp. The cable lengths in automotive environments can be long, and consequently the cable resistance can be significant. For a cable impedance of 20 mΩ, the inrush results in a ~1.5 V drop across the cable for a few milliseconds, (until the bulb is sufficiently turned on). Further, a typical connection to the supply in an automotive environment is switched through protection relays and fuses (housed inside the junction box). These may also present impedance to the inrush and limit the voltage swing available for the operation of high side switch. It is assumed (in this hypothetical case) that this drop is ~ 1V. In addition to losses in the supply line, there are losses in the GND line as well. Modules, in automotive environment, are connected to chassis GND through a resistive network for protection purposes. This network adds to the losses, averaged to ~1V for this example. This implies that losses in the automotive application could easily lead to a 20~25% drop in the supply voltage at a nominal V_{BATT} = 14 V for a readily observed situation of a headlamp turn−on. The high side switch should be able to operate under reduced battery voltages. It should be noted that “operation” in this regard encompasses a fully turned on charge pump, available protection for current limitation (if required) during inrush and a complete diagnosis feature set. Now, consider a bulb turn−on at cold ambient temperatures. At low temperatures, the battery voltage will further droop and the inrush required for the lamp turn on will increase− both these factors create a stringent environment for switch operation. All **onsemi** high−side SmartFETs typically operate well down to 8 V and certain devices also spec an extended battery voltage down to 4.5 V (Refer to specific product datasheets for low voltage operation). Section Under−Voltage Operation describes the LV124 spec and under−voltage behavior.

While the above discussion is focused more on droops in the battery voltage, transient overshoots in the supply voltage are also seldom observed in automotive applications− especially in cases like a jump start, or an alternator load dump (Refer to Section Over−Voltage Protection for details). The high−side switch should be able to protect itself against such events. In case the load is

switched repetitively in a PWM operation, for instance considering the bulb load again where the intensity of light is controlled with a PWM drive, the controller should modulate the RMS voltage across the bulb (by modulating the PWM duty cycle) to minimize fluctuations in the intensity. Another key consideration with the automotive environment is the EMI performance in the system. With increasing electronics content in the modern day automotive applications, every component should be designed while guaranteeing conformance to the required EMI/EMC standards and minimizing the cross−coupled noise both internal and external to an application.

The switching characteristics of a high side SmartFET, therefore, should account for EMI implications as well, in addition to losses. In multi−channel devices, there should be no interference between channels, especially when one channel is reading fault state.

As discussed before, that chassis in an automotive application is considered as system GND, the high side switch should be robust enough to handle and protect itself in case of an output shorted to GND (a highly likely system fault condition in high−side applications). This is usually achieved by limiting the load current and incorporating thermal shutdown (Refer section Short Circuit OUT to GND−Current Limitation and Temperature/Power Limitation for details) in the device. AEC−Q100−012 (Refer [4]) describes the typical automotive short circuit condition set and also quantifies the performance of a device (in terms of number of cycles) against a short circuit event.

The calculations and estimated losses presented in this section above are exemplary and should not be extended as a representative of generic automotive condition set. In general, cable dimensions (and associated losses), power supply distribution fuse/relay specs, ground connections etc. are all OEM dependent, and OEM specifications should be referred to while making a selection for a high−side switch in an application.

Resistive Loads

Typical resistive loads in automotive applications comprise (but are not limited to) LEDs, heating elements in seats, transmission and engine management systems, airbag squibs, air flow sensors etc. LEDs, or Light Emitting Diodes are current controlled loads, −in other words the light output is directly proportional to the drive current, or the input electrical energy. The operation of an LED is very similar to that of any diode; except for the semiconductor material employed for fabrication that emits photons on electronic excitation (quantum of light) instead of phonons (quantum of mechanical vibration)− as in a Si diode. The color output depends primarily on the energy band−gap of the starting material (Refer [1]).

The input drive circuit is controlled through either current regulation or voltage regulation across the LED load. A current is usually limited by stacking multiple arrays of LEDs (within a module) in parallel and adding a limiting resistor in series with the array. A voltage regulation, on the other hand, is typically achieved with DC−DC conversion stages that bring down the voltage required for turning on an array. Figure 4 depicts a parallel cluster of LEDs driven by a high side SmartFET. Each array has n number of LEDs in series. $R_{PROTECT}$ limits the current through the cluster. In case one LED goes faulty and reads open circuit (as highlighted in red in Figure 4), the other arrays will still operate and conduct. The current through the load module, however, will change and the high side SmartFET should be able to indicate this change through analog current sense read−out. Since typical automotive LED loads are driven at low current levels of the order of a few mill− amperes (Refer Figure 5), it is challenging to precisely reflect the small change in current and thereby diagnose an open circuit of a particular LED string. As will be discussed in Current Sense and Diagnostic, the current sense accuracy reduces at small load currents; different design schemes have been implemented in **onsemi** High Side SmartFETs to improve sense accuracy (Refer section Current Sense De−Saturation at Light Loads).

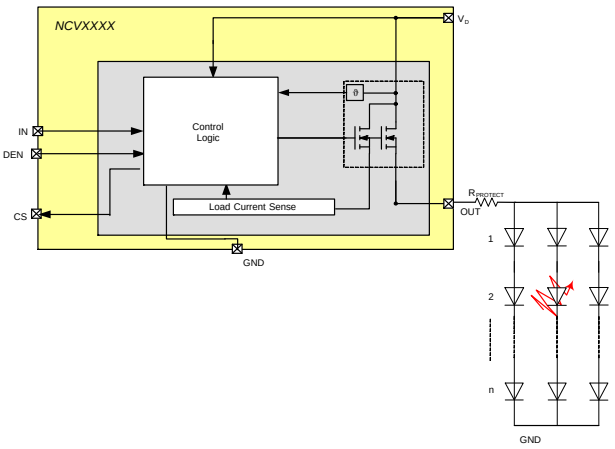

Figure 4. High Side Switch Driving a Parallel Cluster LED Array

Most automotive applications employ a PWM drive scheme to modulate the intensity of output light; the switching characteristics of the high−side switch should be compatible with the application's PWM requirements. Resistive Switching provides the details on LED switching.

LEDs have been gradually replacing the traditional incandescent sources of light for both vehicles' interior and exterior lighting applications. High energy efficiency (proportional conversion of electrical energy into light), better light output (output light is more directional/anisotropic as compared to bulbs that have a diffused output spectrum), ease of drivability (LEDs typically require a low input power and a drive circuit with minimum complexity) and a longer operating life (LEDs do not comprise of a filament, or any internal component that may fatigue over time) are the primary motivations driving OEMs towards LED loads as a viable alternative for automotive lighting. A few shortcomings, for instance, the high initial cost and challenges in achieving an efficient

thermal management (especially for applications like headlight) still need to be addressed. Figure 5 summarizes the typical automotive LED applications and their drive requirements.

Location	Application	Drive Current (Low/Med/High)
Exterior	Center High Mount Stop Lamp	Low (<100mA)
	Side View Mirror	Low (<100mA)
	Side Markers	Low (<100mA)
	License Plate Lamp	Low (<100mA)
	Rear Combination Lamps	Med (200~500mA)
	Turn Signal	Med (200~500mA)
	DRL	Med (200~500mA)
	Head Lights	High(>500mA)
	Fog Lights	High(>500mA)
Interior	Colored RGB Lighting (Including ambient lighting, instrument cluster lighting, LCD Backlighting, Switches, Front Panel (Clock etc.))	Low (<100mA)
	Map/Dome Lights	Med (200~500mA)

Figure 5. Typical Automotive Applications Utilizing LEDs

Inductive Loads

Inductive loads mostly include different motors in applications such as wipers, starters, door modules, HVAC, fuel injectors, electric power steering, throttle control etc. In addition, there are relays used in engine and body control applications. While driving inductive loads, the primary concern is to limit the magnitude of the output voltage when the inductor begins to discharge. All **onsemi** High Side SmartFETs have an integrated protection clamp for this purpose. The mechanism of active clamping is explained in section Inductive Switching. Another concern with the inductive loads is the inductive discharge energy capability of the high side SmartFET. The product datasheets specify the single pulse and repetitive pulse energy capability across a range of inductors at defined starting ambient temperatures (Refer section Inductive Switching for equations describing the energy dissipation in the high side switch). Exceeding the energy rating may irreversibly damage the device. The protection features will not be active once the input command is turned to trigger inductive flyback.

To protect the device from high energy dumps during inductive discharge, some applications employ a free−wheeling diode and external clamping. Figure 6 shows two such options marked inside the dashed red rectangles. A series L−R load is depicted because all inductive loads have an associated parasitic resistance. While paralleling across the load, the available voltage to discharge the inductor is just a diode drop, which may lead to a prolonged discharge. The clamp voltage in the second option will depend on the breakdown of the external diode (the breakdown should be lower than that of the integrated clamps within the device). In both cases, the diode should be capable of handling the power dumped in the inductive discharge. While implementing these designs, extra components may be required to protect against reverse battery conduction, overvoltage scenarios etc.

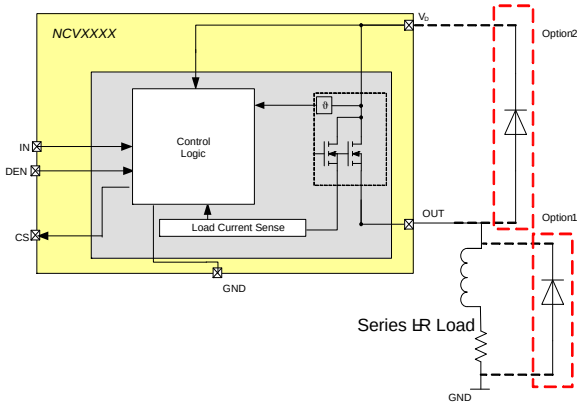

Figure 6. High Side Switch Driving a Parallel Cluster LED Array

It should be noted that the clamping schemes described above are only indicative. Other circuit configurations with external clamping may also be used. However, detailed calculations of power handling capabilities of the external components, analysis of protection during reverse battery and overvoltage situations as well as estimation of the associated leakage levels should be done before employing these topologies.

Bulb Loads

An incandescent bulb is very different in operation than the LED light sources discussed in section Resistive Loads. The bulb comprises of a tungsten filament in a glass enclosure filled with inert gases such as argon or xenon, for instance. The contact wires carry current in and out of the filament supported by mounts and caps for mechanical support and casing. When an electric current is forced through the tungsten filament, the temperature of the filament increases and eventually it starts to glow thus emitting light. Most of the input electrical energy is converted into heat and rest is converted into light. The light conversion efficiency of incandescent lamps is inferior to that in other light sources like LEDs, CFLs etc. However, a low cost of manufacturing and availability across different power ratings make it the most widely used light source in the present day automotive applications.

The electrical behavior of a bulb is capacitive, with the high current required in the beginning for heating the filament gradually decaying to a nominal current required for operation. This initial high current is called the bulb inrush. The resistance presented by a “cold” bulb (the term cold describes the initial turn on, or the inrush) is lower than that in a steady state operation. The steady state resistance depends on the desired final filament temperature (For most bulbs, the desired filament temperature is 2900~3200 K). Describing the closed loop electro−thermal operation of a bulb: On the application of an electrical voltage source, the

current across the bulb depends on the dynamic resistivity of the filament (which is a function of temperature). The instantaneous temperature of the filament depends on its thermal resistance (and the thermal resistance of the contacts) and the input power (which in−turn depends on instantaneous current), thereby making it an iterative model. There are various models that predict this closed loop resistivity profiles using look−up tables or empirical equations (Refer [2]).

Typically, automotive lamps specify a rated power at a nominal voltage. The nominal resistance of the filament can be calculated as:

$$R_{NOM} = \frac{V^2_{NOM}}{P_{NOM}} \quad \text{(eq. 1)}$$

where V_{NOM} and $_{PNOM}$ are the rated voltage and power. Based on empirical data, the dynamic resistance can be estimated as a function of instantaneous temperature using an “inrush factor”:

$$R(T) = R_{NOM} \cdot \left(\frac{T_{REF}}{T}\right)^{const} \quad \text{(eq. 2)}$$

T is the instantaneous filament temperature, T_{REF} is the desired filament temperature and “*const*” is an empirical constant (Refer [3]). The latter part of the multiplier in Eq. 2 is the inverse inrush factor. The inrush current profile can be simulated using the dynamic resistance profile assuming a known stable voltage across the bulb.

Figure 7 below lists the applications widely using incandescent bulbs along with the rated power of the bulbs.

S.No	Application	Rated Wattage
1	Front Light (High Beam and Low Beam)	51W; 55W;60W;65W;60/55W*
2	Parking Light	Front: 4W; 5W; 6W Rear: 10W; 21/5W*, 21/4W*
3	Turn Signal Lights	Door Integrated: 4W; 5W Front and Rear: 21W
4	Reverse Lights	16W; 21W
5	Warning Lights	21W
6	Brake Lights	CHM: 5W;16W Rear: 21W; 21/4W*; 21/5W*
7	Trunk Light	5W
8	Fog Lights	Front: 55W; 35W Rear: 21W
9	Interior Lights	3W; 5W; 10W; 15W; 18W
10	License Plate Lights	4W; 5W
11	Daytime Running Light	35W; 55W
* Two Filament Bulbs		

Figure 7. Typical Automotive Applications Utilizing Incandescent Bulbs

It is critical to understand the output current drive capability of the high side switch with respect to the inrush profile required for the application bulb. **onsemi** High Side SmartFETs are equipped with the current limitation feature to protect themselves in case of overload situations (Refer section Short Circuit OUT to GND−Current Limitation). Extended operation at the current limit forces the device to repeatedly turn off and on because of the thermal shutdown mechanisms (Refer section Temperature/Power Limitation). While such protection is desirable to limit the transient thermal stresses in case of system failure conditions such as output short circuit to GND, the bulb turn−on characteristics are impacted if the inrush required for the bulb turn−on is greater than the internal current limit. In such case, the device attempts to turn on the bulb with a re−try strategy (refer section Re−try Strategy). The idealized wave−set in Figure 8 and Figure 9 depicts the bulb turn−on scenario with and without the re−try strategy.

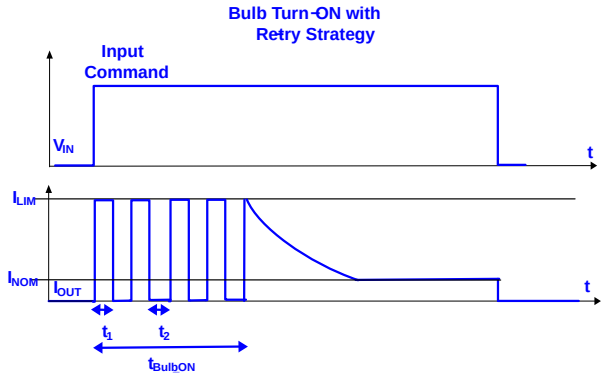

Figure 8. Bulb Turn−On With Retry Strategy

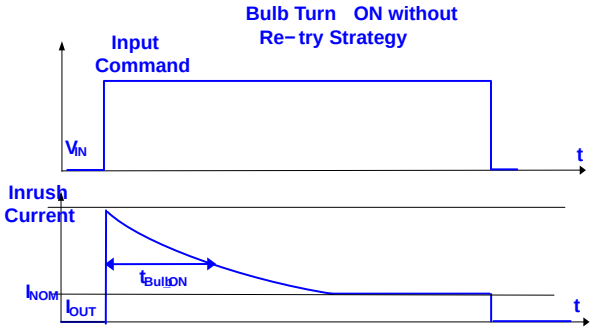

Figure 9. Bulb Turn−On Without Retry Strategy

Referring to the waveforms above, t_{Bulb_ON} is the time required to turn on the bulb− in most cases, it is the time interval in which the instantaneous current drops to ~0.5* peak inrush current. The specifications for this parameter are OEM dependent. With internal current limitation, t_{Bulb_ON} increases as the device toggles in and out of differential thermal shutdown. The root mean squared current over the I_{LIM} cycles and the consequential power at the beginning of the last re−try should result in an equivalent electro−thermal resistance profile (of the bulb) as in the case with no re−try after a period of t_{Bulb_ON}. While selecting a device for an application, it should be considered that t_{Bulb_ON} in the worst case condition (typically in case of low ambient temperatures when a high inrush is required at low available battery voltages) should be within the limits defined by the OEM. Measured maximum inrush currents for certain standard automotive bulb loads have been tabulated in Figure 10. Measurements were performed by

forcing a stable differential voltage of ~12.8 V across the bulb (For an accurate inrush profile, the voltage across the bulb should be stable, any parasitic resistive drops in the measurement system may yield a low inrush current because of a reduction in the voltage available to turn the bulb on). The maximum inrush depends on the electrical specifications (primarily, electrical wattage) and the physical construction of the bulb. The injected power in the bulb is dissipated as conducted power across the filament and the radiated power. The physical structure of the bulb determines the distribution of power and thereby also impacts the instantaneous temperature and inrush profiles.

Bulb	Spec Voltage (V)	Spec Power (W)	Max Inrush @ 25C (Amp)	Max Inrush @ -40C (Amp)
W3W	12	3	2.24	2.95
T4W	12	4	3.69	4.77
R5W	12	5	4.51	5.79
H6W	12	6	7.46	9.83
R10W	12	10	9.81	12.77
P21W	12	21	23.64	31.67
P27W	12.8	26.9	22.01	28.75
H1	12.8	55	63.67	82.73
H4	12.8	55	71.77	89.80
H7	12.8	55	62.99	81.68
HB2	12	60/55	78.30/70.07	98.75/90.19
HB3	12	60	72.00	92.41
H9	12	65	70.50	91.03

Figure 10. Measured Maximum Inrush For Typical Automotive Bulbs @ V ~ 12.8 V

It should be noted that measured bulb inrush are only typical and do not represent the extremes of variations in the bulb performance. In addition, the inrush profiles may vary across bulb manufacturers. Devices recommendations (against specific bulbs) can be provided on customer requests.

Relay and Fuse Replacements

There has been evident focus on component weight and size reduction in all automotive applications in order to achieve higher system efficiency. Also, with extensive electrification in vehicles, there has been a growing requirement to replace existing switching and protection components with solid state solutions. Towards this objective, various **onsemi** High Side SmartFETs are targeted at replacing application relays (relays are usually heavier and consume a significant area on the PCB). It is recommended to refer to the product datasheets for specific suitable applications. In addition, the ultra−low ohmic devices (with typical $R_{DS(ON)}$, for instance, between 0.5~3 mΩ) are targeted to replace protection fuses and offer an E−fuse solution. The smart high side switch creates a closed loop protection scheme with fault reporting and the integrated protection features protect the E−fuse from getting damaged− thereby reducing the replacement cost (over vehicle's lifetime) associated with the fuses.

While the relay and fuse replacing SmartFET solutions utilize the standard set of features available across the portfolio, there are some key application requirements that differentiates the design approach for these SmartFETs from those switching other conventional loads such as lighting, or resistive elements. A few instances of these differentiating requirements include the difference in retry strategy in case of a short circuit to ground, current sense ratio specs, operating temperature range, number of output channels, reverse battery protection, slew rates etc. Most of these requirements would be discussed individually in the respective sections to highlight the required adaptability in design as the market impetus shifts progressively towards power distribution using smart switches.

Functional Safety Overview:

With the advent of smart switches in more safety critical applications such as SRS (Secondary Restraint Systems, including airbags, pre−tensioners and braking), power distribution and transmission, among others, due consideration and adherence to functional safety standards has been more important than ever. Standards such as ISO26262 elucidate a designer's approach to incorporate features while conforming to safety functions described in the standard. It should be noted that the emergence and application of these standards is recent which makes it difficult for the semiconductor manufacturers across industry to re−design their products in hindsight. To address this predicament, **onsemi** provides product specific (on customer request) Failure Mode Distribution Analysis, design and package specific FIT rates, and block wise impact on safety functions in the form of an open FMEDA. Further, these FIT rates are provided based on multiple standards−such as IEC 62380, SN29500 etc. understanding that different standards may be employed across customers for analysis. This information helps the customers design the system with the necessary failsafe mechanisms built in for safety critical applications per the desired mission profile over the intended lifetime. For specific functional safety requests, it is recommended to contact the respective field representatives.

POWER FET AND PROTECTION

Power MOSFET

This section describes the structure and different topologies of the power element, or the DMOS. The power element in a high side device is comprised of a large number of vertical N−channel FET cells laid out in parallel with the drain as the substrate for an improved heat spreading and reduced thermal density over the drain area. Optimal design and area considerations of the power FET are critical in determining the key electrical performance metrics including, but not limited to, $R_{DS(ON)}$, max current capability, breakdown voltage, current sensing, temperature sensing etc. Based on technology, parametric requirements and geometrical constraints, a "planar", or a "trench" configuration could be employed in **onsemi**'s high−side SmartFETs. Following is the depiction of the two structural designs.

Planar vs Trench FET

As discussed above, the vertical power element may be planar, or a trench structure. The terms “planar”, and “trench” here, refer to the Gate Stack Structure which consists of the poly gate, underlying oxide and the channel. The former design has a planar, or a lateral gate and channel with near surface channel conduction, while the latter design has a vertical Gate and channel going into the depth of the body (See figures 11 a) and 11 b) for details).

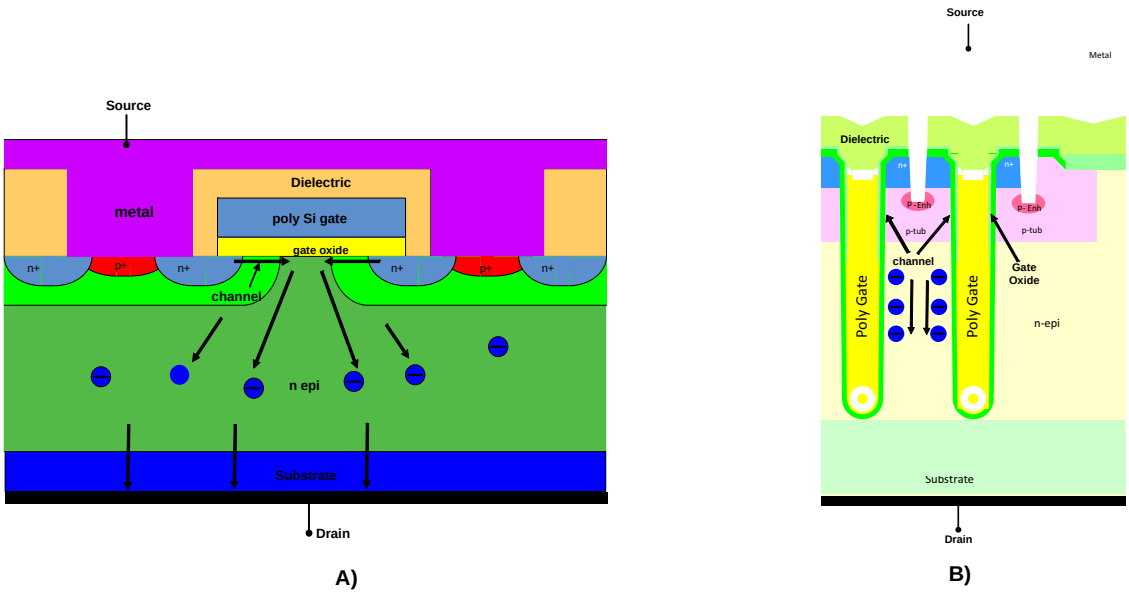

Figure 11. Exemplary Layout Depicting the Gate, Channel and Carrier Flow in a) Planar FET and b) Trench FET

The conventional, or the planar FET is thermally efficient and easy to manufacture with low “mask steps”, while the trench counterpart offers a tighter cell pitch (resulting in better specific $R_{DS(ON)}$) yielding the ability to pack more cells within the given chip “real−estate”. The following table summarizes the key differences in the two designs, differentiating the performance as Hi (Good), or Lo (Moderate) against a specific characteristic.

Table 1. PERFORMANCE COMPARISON IN PLANAR AND TRENCH VERTICAL POWER FETS

Parameter/Characteristic	Planar FET	Trench FET
Specific RDS(on) − mΩ *mm2	Lo	Hi
Thermal Stability	Hi	Lo
Energy Capability for Similar FET area	Hi	Lo
Ease of Manufacturability	Hi	Lo
Cell Pitch	Lo	Hi

Monolithic vs Dual Die Technology

A monolithic high side device has the power element (vertical N−FET) and the control circuit fabricated on the same substrate/starting Si. The term “dual die”, on the other hand, refers to having two separate die for power FET and controller within the same package. A monolithic design renders least mismatch and offsets between the FET and the controller; however, at sufficiently low specific $R_{DS(ON)}$ levels with a complex control circuitry comprising of analog and digital sections, it is challenging to monolithically integrate the two elements (FET and controller) within a given package size. This is where technologies like chip−on−chip are utilized to optimize the “package real−estate”. Further, the control circuit needs to be fully isolated from the FET using isolation structures. Following (Figure 12) is an exemplary representation of a monolithic high−side device. Bond pads to the controller and power FET, and various sense elements (Temp Sense, Current Sense) are also shown in the die image below.

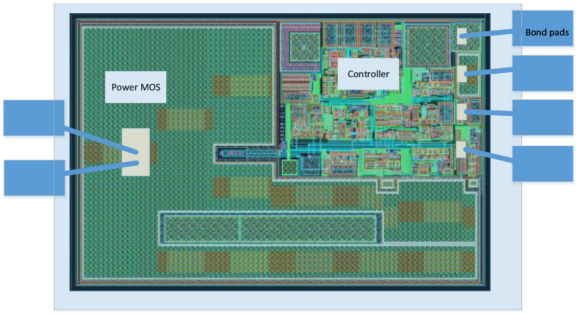

Figure 12. Representation Of a Monolithic High−Side Smart FET Design

It should also be considered that while most of the high−end SmartFET control circuitry is based on CMOS

logic, it is always challenging to incorporate a back side drain technology in a monolithic configuration with isolation between CMOS substrate and back side drain.

A dual−die technology manages the interaction between the FET and control circuit through inter−die bonds which require additional front−end masking, sacrificial die area for bonding, and back−end assembly and processing steps. Because of different starting silicon for the two elements, there are some inherent process mismatches associated with dual−die technology devices. Figure 13 depicts a high level block diagram representation for such technologies.

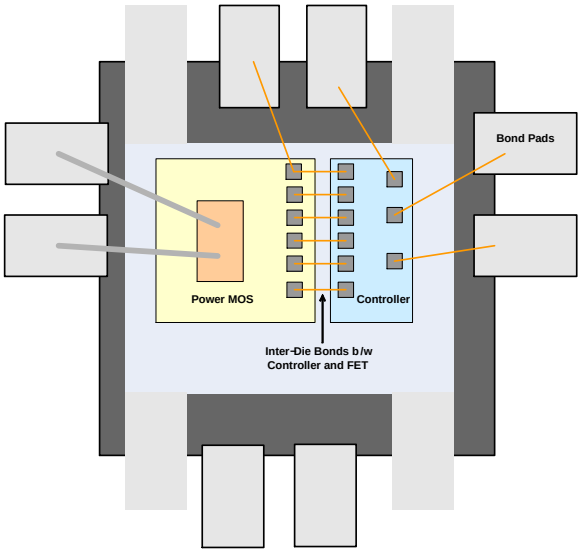

Figure 13. Representation of a Dual−Die High−Side SmartFET Design

The advantage with this technology is the ease in substitution of FETs with different sizes and $R_{DS(ON)}$ levels while maintaining the compatibility with the controller across a specific product family.

Depending on the application requirements, and product family segment, **onsemi** High Side SmartFETs could be fabricated on either of these technologies.

Multi−Channel Devices

Some applications require multi−channel devices for operating parallel loads (Refer section Application System Overview). Such devices are required to have independent power N−FETs with identical parametric and behavioral performance. Each power FET, or “channel”, has its independent sensing elements, and the diagnostics are typically multiplexed. A challenge with these devices is to isolate the operation of the two channels, especially in case where one of the channels is in a fault condition. Figure 14 below presents a circuit schematic detailing different blocks in a dual channel High−side device, for instance.

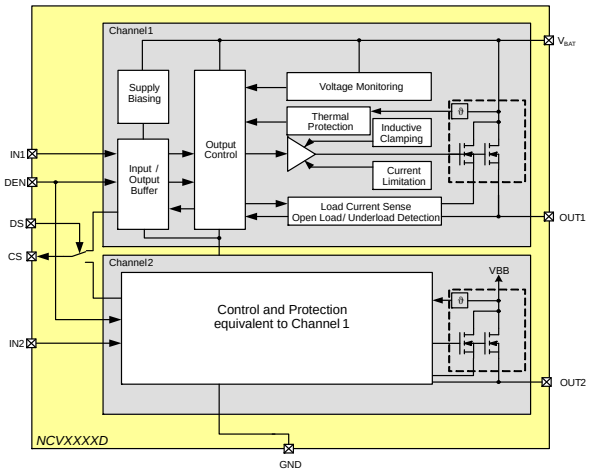

Figure 14. Example Circuit Block Diagram for a Dual Channel High−Side SmartFET

Charge Pump−Principle of Operation

An efficient charge pump design is extremely critical to achieve the desired performance from a High−Side FET. To make sure the FET is fully turned on in the $R_{DS(ON)}$ region (of the output characteristic curve), the gate potential needs to be boosted over and above the battery (drain potential) to provide sufficient overdrive to the N−FET. A charge pump, as the name suggests, essentially acts as this boost circuit and ensures maximum $R_{DS(ON)}$ for a given die area. Though, in a strict definition, a charge pump is integral to the control circuit, however, since its characteristics are directly tied to the performance of the power FET, it is being discussed in this section.

In addition to generating sufficient gate charge, an efficient charge pump must provide a stable gate drive with smooth turn on and turn−off characteristics, and should be realized on a minimum die area. Typical charge pump networks employ stages of switched capacitor boost networks, though; this is not the only method to generate high voltages.

Figure 15 is a block diagram representation of a charge pump operation. Based on the command from the input control circuit, an oscillator produces a set of “de−phased” output signals which then are fed into the boost network as shown in the figure on the right. These signals control the switches and charge the capacitive ladder. The difference in the phases results in accumulation of charge/generation of high voltage at the output of this network.

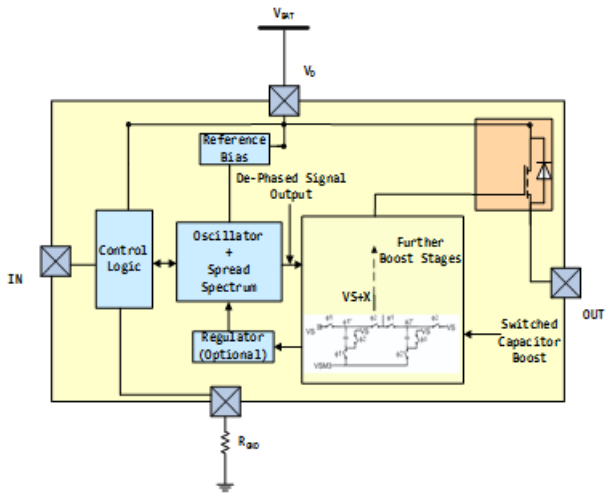

Figure 15. Charge Pump−Operational Block Diagram

A charge pump output may be regulated to make sure there are no gate voltage overshoots by pulling back on the booster, once the device is closing into complete turn−on. This may increase the time to achieve the full−scale gate overdrive required for the $R_{DS(On)}$, but improves the gate control stability and reduces overshoots.

In some devices, oscillator frequency is trimmed in production. This ensures tight tolerance across population around the nominal switching times specified in the datasheet. Different technologies (within the **onsemi** High Side SmartFET product portfolio) may or may not have an internal regulator. Depending on the gate potential required, the boost stages can be cascaded to multiply the charge at each stage.

The internal spread spectrum is used along with the oscillator to suppress any spectral energy spikes produced by the oscillator, and ensures good EMI performance. It should be noted that switching speed of the device is also contingent on the rate at which the charge pump can boost the gate voltage and how fast can the gate be “unloaded”. While it is desirable to have a fast charge pump response, it should be designed in a way not to infringe with the EMI requirements.

Supply Voltage

Typical Supply Voltage Specs

onsemi High−Side SmartFETs have been designed to operate across typical battery voltage range for an automotive environment accounting for application variations around the nominal value as described later in this section. The operating voltage range is typically specified as 5 V −28 V, however, some specific datasheet parameters may be characterized and guaranteed across a narrower range, for instance 8 V to 18 V. The range and the corresponding electrical specs guaranteed will differ across devices and technologies within the **onsemi** High Side SmartFET portfolio. Following is a depiction of a typical supply voltage spec.

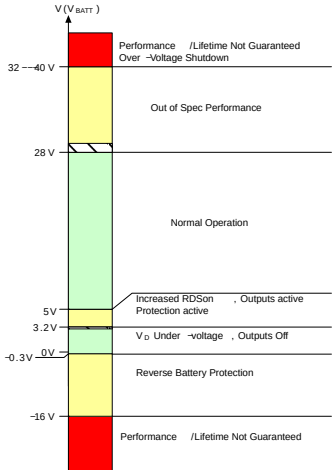

Figure 16. Device Operation Across Typical Supply Voltage Specification

As described in the chart above, the normal operation is guaranteed (unless otherwise specified in the product datasheet) across a range of 5 V – 28 V. The electrical performance (in terms of typical $R_{DS(ON)}$, switching speeds, current sense etc.) and expected behavior (in terms of protection and diagnostics) may deviate out of spec outside this range. Below the under−voltage threshold, the device turns off and turns back on with a hysteresis. Reverse Battery protection for controller and FET, as described later in this section, is achieved through internal clamping structures and the body diode respectively. Reverse battery threshold for typical devices is −16 V (sustained for a defined time interval), below which, the expected lifetime, reliability and performance may be irreversibly affected. Some devices may employ an over−voltage shutdown feature to prevent the FET and controller from high voltage transients observed during events like a Load Dump; other devices offer over−voltage protection through internal clamp structures, and lifetime/performance of the device may be compromised if operated in this high voltage region. The over−voltage shutdown threshold may be different across devices.

Under−Voltage Operation

onsemi High Side SmartFETs have an under−voltage shutdown mechanism when the supply voltage droops too low to support device operation. This feature also prevents the device from flagging any false/out of spec outputs or diagnostic signals. The under−voltage threshold differs across devices with typical spec in the range of 3 V~ 4 V. An under−voltage shutdown event has an associated hysteresis to prevent aberrant turn on and turn off because of a potential noisy power source in the vicinity of threshold.

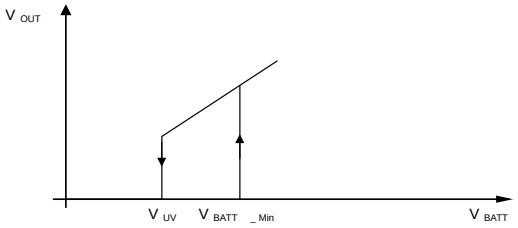

Figure 17. Under−Voltage Turn Off With Hysteresis

Such low voltage events are most likely observed in an automotive environment in case of cranking (vehicle starting) conditions when the battery voltage can fall to a low value for a brief event before rising eventually. The difficulty is compounded in case of “cold cranking” when the battery voltage further droops at low ambient temperatures. As per the LV 124 automotive spec for electrical and electronic components in motor vehicles up to 3.5 tons, the supply voltage trajectory while cold cranking is described in the following wave−set.

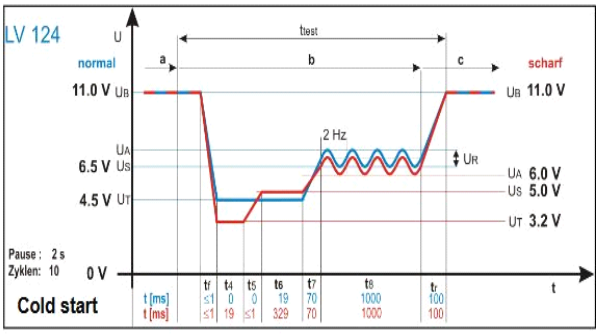

Figure 18. LV124 Spec−Battery Voltage Trajectory During a Cold Start Event

The worst case low voltage per this spec 3.2 V. Certain **onsemi** High−Side devices like NCV84012A comply with this standard, while devices such as NCV84160 have under−voltage shutdown triggered at 3.5 V slightly above the minimum voltage spec of 3.2 V. The output and diagnostic behavior in an under−voltage event is described in Figure 19.

Some of the low $R_{DS(ON)}$ higher power SmartFETs have an under−voltage recovery delay timer designed in. This feature helps protect the device when an under−voltage condition is triggered consequential to the battery voltage pulled down (by its output impedance) in a high current conduction scenario such as short circuit current limit. Once the device safely shuts down and the current decays, the battery voltage rises again. In the absence of the alluded feature, the device will turn back on again into the short circuit as $V_{BATT} > V_{BATT\_MIN}$, overriding the built−in cool down time (Refer section Short Circuit OUT to GND − Current Limitation). The repetitive retries can be stressful for the die especially in case of high current devices observing a persistent short circuit. Incorporating a delay timer, spaces out such retries and allows the die to “cool down” sufficiently before the next retry. Figure 20 explains this phenomenon. Refer to product datasheets for details on UV delay specification.

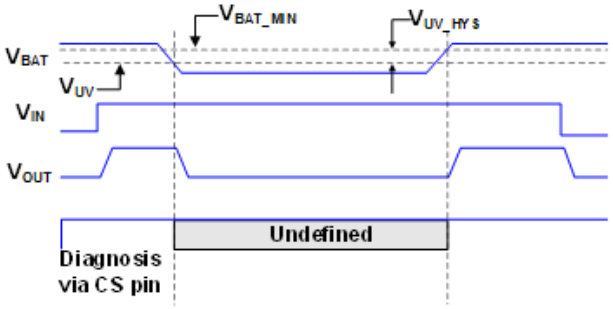

Figure 19. Idealized Wave−Set Depicting The Device Behavior During Under−Voltage

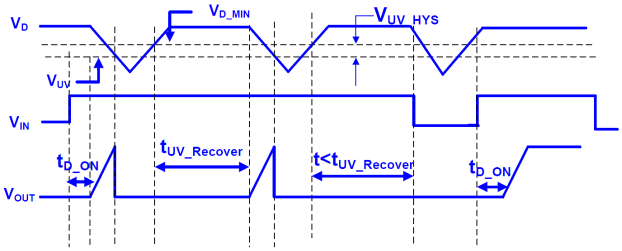

Figure 20. Under−voltage Recovery Delay

Over−Voltage Protection

Over−voltage scenarios, in an automotive environment, primarily occur because of high voltage transients conducted/coupled across the supply line (including alternator load dump), electro−static discharge (ESD) and jump start events. In a load dump event, the battery connection to the alternator (which provides the charging current to the battery) is lost, and the output current becomes unregulated, and thereby the loads connected to the alternator observe a significant increase in the supply voltage until the alternator regulator responds and cuts back on the drive current. A vehicle manufacturer specifies the characteristics of the load dump pulse by defining the voltage and time period for this pulse. In addition, standards like ISO 7637−2: Electrical Transient Conduction Along Supply Line Only (Refer [5]), also define specific ISO pulse profiles and load dump test cases. Over the recent years, the use of transient voltage suppressors at the alternator have led to the relaxation of load dump requirements in the form of a “suppressed load dump” spec (typically around 35 V for 12 V applications). This has allowed for scaling down the feature size on the die facilitating low $R_{DS(ON)}$ devices in shrunk packages such as NCV84012A. In case of a jump start, the vehicle battery is being charged by a high voltage source to start the engine, for instance, the battery of a truck, or a double car battery (usually to compensate for the line losses in the long charging cables). For a jump start, again, the pulse characteristics are defined by the OEM. A jump start event is less stressful than a load dump condition. Most automotive loads are required to sustain these high voltage events as specified by the OEM. **onsemi** High−Side SmartFETs have internal clamp structures designed to protect the FET and the controller against high voltage spikes.

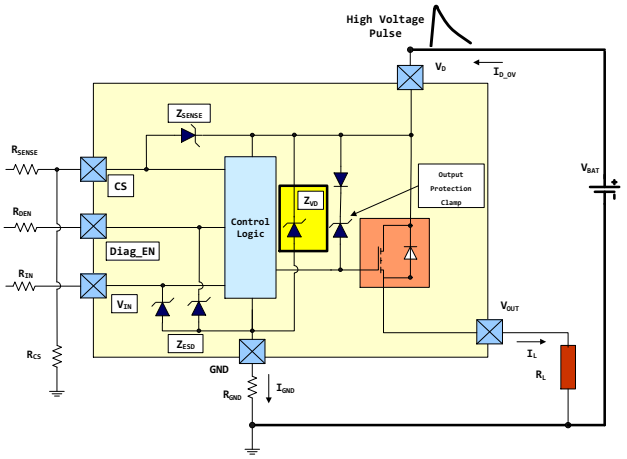

Figure 21. Schematic Representation of Over−Voltage Protection Clamp Structures in a High Side SmartFET

Referring Figure 21, there is a protection clamp for the power FET from Drain−Gate that limits the voltage swing at the output. In case the FET was initially off, this protection clamp conducts if the voltage at the drain terminal exceeds the zener breakdown, and turns the FET on by developing a potential across the Gate−Source impedance. The load impedance at the output limits the current through the FET. If the FET was initially on, it will stay on unless the device incorporates an over−voltage shutdown, as mentioned in section Typical Supply Voltage Specs. A separate clamp structure limits the voltage drop across the control section to Z_{VD}, and the ground impedance network limits the current through these clamps. The protection diodes at the logic inputs clamp these inputs to a diode below the GND potential. The protection clamp for current sense, Z_{Sense} in High−Side SmartFETs is referenced to the supply rail. As a standard practice, **onsemi** recommends external clamps at the current sense output to limit the voltage observed at the input A/D stage of the microcontroller. Also, it is recommended to have external protection resistors at the I/O pins interfacing with the microcontroller to prevent the microcontroller clamp structures from excessive current. An extended operation in the high voltage regime may impact the lifetime, robustness and performance of the device.

Device layout, terminations and metal routings are also carefully designed for superior transient high voltage robustness. The devices are subjected to standard ISO pulses and rated on the max ESD transient capability per the human body model and machine model (Charge Device Model Ratings are also provided for certain devices). Refer to product datasheets for specifications.

Inductive Flyback

While switching an inductive load, the voltage at the output terminal may observe a considerable negative swing dependent on the rate of current decay at device turn off and the effective inductance being discharged. The Drain−Gate protection clamps limit the magnitude of this swing and provide an “active clamping” of the output potential to $V_{BATT} - V_{CLAMP}$, where V_{BATT} is the drain potential and V_{CLAMP} is the breakdown voltage of the protection clamps. Active clamping reduces the stress inflicted on the clamp diodes and improves the heat dissipation during inductive discharge by distributing the current density though the entire FET area. Such an approach is preferred over a scenario where the back−side body diode avalanches (i.e. breaks down) and discharges the inductor. For further details on the output behavior, clamp functionality and inductive energy capability, refer section Inductive Switching.

Loss of Power Supply

If the supply connection to the drain terminal is lost, a High−Side Smart FET protects itself by disabling the power device and the control section. Both OUT and Current Sense read “Lo” during a loss of supply event. In a case where the connection to the supply is lost during inductive switching (or if the wiring harness is sufficiently inductive), there has

to be a flyback path for the current to be discharged. This path would include the protection diode for the control section (Z_{VD}, see Figure 19) limited by the external ground resistor. Since the protection diodes are not as capable as the power FET to handle the inductive flyback energy, this may damage the High−Side Device in cases of high energy dissipations. In such cases, due considerations in system design should be given, for instance, by including freewheeling diodes to provide a path for the current flow during inductive discharge.

Short Circuit to Power Supply

A short circuit to power supply event is depicted below.

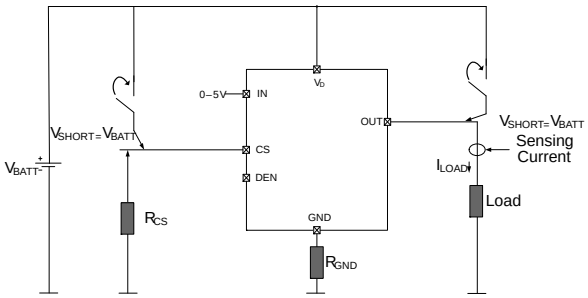

Figure 22. A Short Circuit Event to Power Supply

The above figure describes the short circuit of V_{BATT} line to the two output terminals− OUT or CS. In the former case, the load will conduct irrespective of the input command. Assuming that the drain terminal is strictly tied to the battery (i.e. no potential drops between battery and drain connections), there is no power dissipated across the device, but the event could be severely stressful for the load. The idealized set of waveforms in Figure 23 describes a transient OUT short to V_{BATT} event occurring in case of a typical bulb inrush. Load current and voltage increases transiently; V_{SENSE} drops to zero because the FET will be off during this time. In Figure 22, it is to be noted that the current is being measured close to the load and does not represent the output current coming out of the OUT terminal (which would be zero in a SHORT to V_{BATT} event).

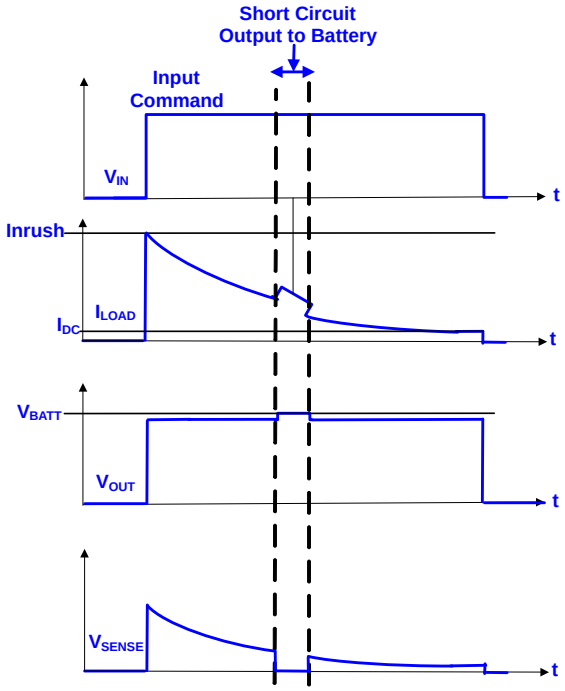

Figure 23. Idealized Wave−Set Describing OUT Short to V_{BATT} Event

If there is an impedance path between battery and drain connections, it may be possible that the source potential (in a short circuit to V_{BATT} event) is higher than drain's, resulting in an inverse current through the body diode. Such a situation, though unlikely in an automotive environment, can be very stressful for the device.

In case of V_{BATT} short to Current Sense, the OUT terminal and the load will operate normally, however a voltage equal to V_{BATT} will be observed at the CS pin which could potentially stress the I/O interface of the microcontroller's A/D. As described in section Operational Methodology, it is always recommended to put in external clamps at the CS pin to prevent high voltages at this node. Figure 24 shows the behavior of OUT and Sense nodes in case of CS short to V_{BATT}.

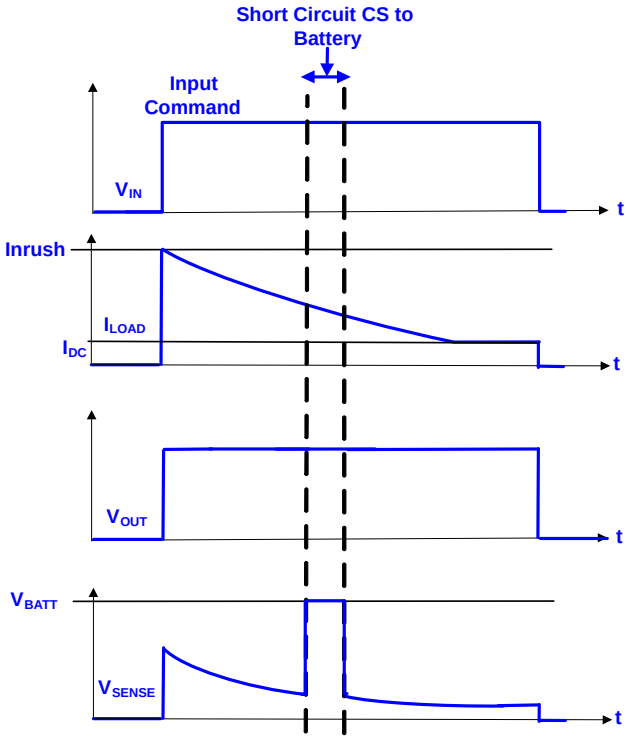

Figure 24. Idealized Wave−Set Describing CS Short to VBATT Event

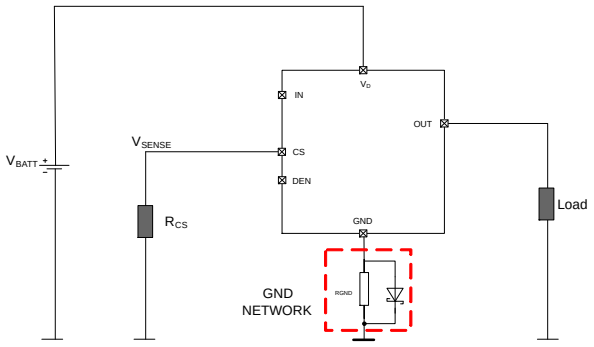

Figure 25. Schematic Representation of Ground Network in an Application

Ground (GND) Operation

Recommended GND Circuit

Understanding and employing an optimal ground network is imperative in an application involving High−Side FETs. As a standard practice, it is not recommended to tie the device GND pin directly to the vehicle, or chassis GND. As explained later in this section, this protects the High−Side FET under some specific system failure conditions. A typical ground network has been highlighted (in red) in Figure 25 − a resistance connected in parallel with (optional) diode. The resistor a) limits the current through the protection clamps, Z_{VD} (see Figure 21) in case of an overvoltage event, b) prevents the power dissipation in the device in case of a reverse battery connection (the protection clamps are forward biased in a reverse battery connection, see Figure 26), or in case of loss of battery during an inductive flyback.

While the resistance does offer device protection, it also raises the GND potential depending on the device's operating GND current. This potential, if high enough, can alter the threshold of the power FET and also limit the headroom rail available for the operation of the analog circuitry within the control section. There is, therefore, a tradeoff in the selection of this resistance. A high value for this resistance implies a low limiting current during over−voltage/reverse battery connections, but would also raise the ground potential significantly.

The diode helps in reducing the GND potential by shunting the resistance during normal operation, and also blocks the reverse voltage (upto its breakdown). It, however, does not help during an over−voltage situation. Unless otherwise suggested, as a typical value, a 1 kΩ resistor is recommended to be used in parallel with a diode, or a standalone resistance of ~150 Ω can be used as the GND impedance. For device specific recommendations, refer to the corresponding product datasheets.

Reverse Battery Protection

When the polarity/connection to the battery terminals is flipped, a reverse current would flow through the device as depicted in Figure 26. The protection diodes and resistors along with the direction of reverse current have also been shown in this block level schematic. The intrinsic body diode of the power FET would conduct a current I_{REV} and the power through this diode is limited by the load itself. In the control section, a ground current, I_{GND_REV} is conducted by the forward biased overvoltage protection clamps, Z_{VD};

I_{IN_REV} and I_{DEN_REV} conduct through the internal microcontroller network into the protection resistors R_{IN} and R_{DEN} respectively. These currents flow through the ESD zener clamps for the digital inputs and eventually add to the current across Z_{VD}. The resistors at the logic inputs, R_{IN} and R_{DEN}, limit the current through the ESD structures; and the ground resistor represented by Z_{GND}, limits the current, and hence, the power dissipation across Z_{VD}. A reverse current, I_{CS_REV} flows into the CS pin through the sense resistance R_{CS} and is fed back into the negative terminal of the battery through the forward biased overvoltage protection diode Z_{SENSE}.

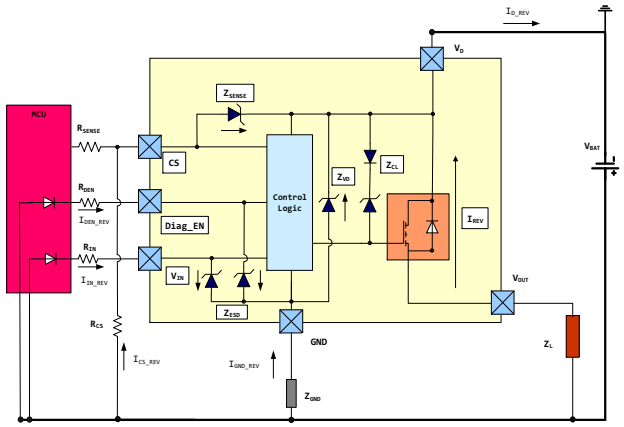

Figure 26. Current Flow and Protection During Reverse Battery Operation

Low−ohmic devices intended primarily for relay and fuse replacement applications, such as NCV84008A, NCV84004A etc. , are equipped with a ReverseON feature that turns on the output FET in an upside down configuration when a reverse battery voltage is observed. Such an operation helps reduce the power dissipation in the device by shunting the body diode and limiting the conduction losses in reverse mode. Fig. 27 highlights the conduction path through the FET instead of the body diode. Further, a reverse battery blocking mechanism in the ground path ensures a low GND current (Refer to specific product datasheets for max allowed reverse battery spec) and allows to undersize the external GND resistor.

In addition to ReverseON, the certain devices also offer an InverseON feature in which the body diode conduction is once again shunted and over−riden by FET turn on if the source potential exceeds that at the drain. Such a condition could be prompted when the output of the FET observes a hard short circuit to battery in the application as explained in the section Short Circuit to Power Supply**.** The $R_{DS(ON)}$ offered by the FET in case of reverse battery, or inverse current conduction is specified in the respective product datasheets.

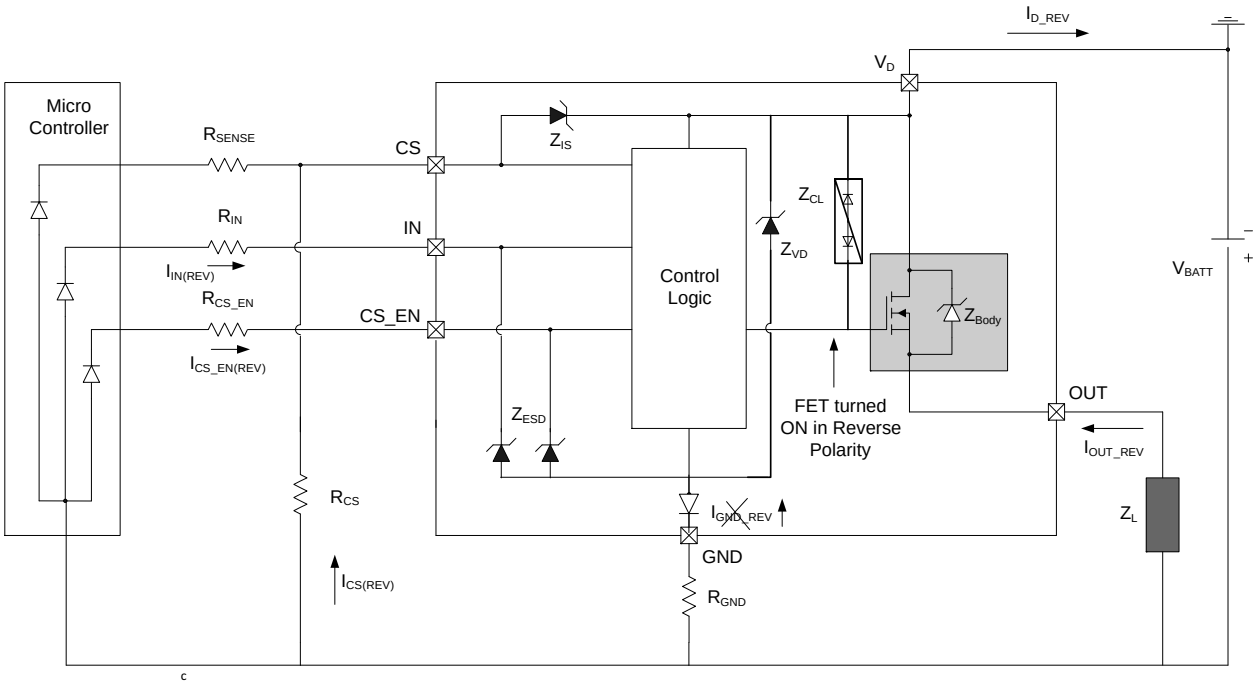

Figure 27. Reverse Battery Protection with ReverseON

It is to be noted that the reverse current in the output stage is not “blocked” in either of the cases described above; rather, the power dissipation is limited by employing FET conduction along with external protection resistors. Certain applications such as fuse and/or relay replacements require an external reverse battery blocking mechanism in the power path to prevent any current conduction in case of reverse battery connection to protect the loads downstream. For the maximum capability of a device (in terms of maximum time and reverse voltage withstood) in reverse polarity mode, refer to specific product datasheets. For loads requiring a reverse current blocking, special care must be exercised (for instance, incorporating reverse battery blocking circuit elements) while working with these High−Side devices. None of the protection features are available in the reverse battery mode.

Loss of Ground

When the GND (Ground) connection to the device is lost, it will turn OFF the output FET and the control section. A loss of GND could occur at the module level (where the connection of the module GND to ECU GND is lost), or at the ECU level− where the entire ECU, including the microcontroller, loses the connection to the chassis GND. In both the cases, there is no return path/reference available for the control circuitry in the device. Any parasitic GND connections to the module should be avoided in the ECU design.

The block diagram below depicts such a situation.

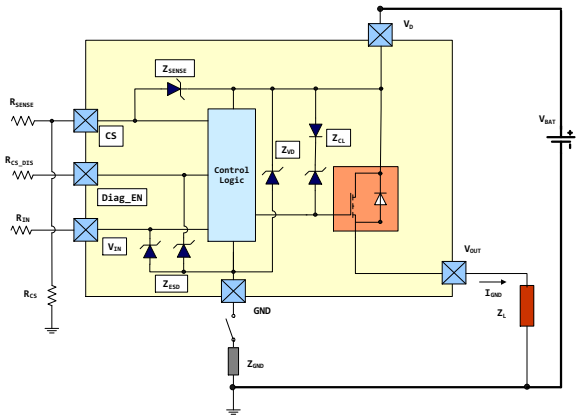

Figure 28. Block Diagram Depicting a Loss of GND Situation. The Load Remains Connected to the Chassis GND, However, the Module GND is Lost.

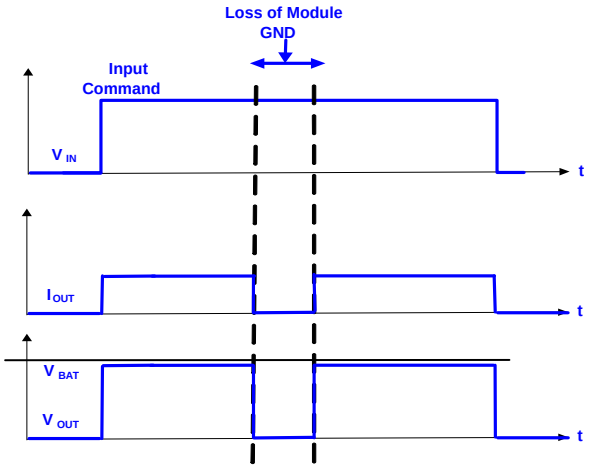

Figure 29. Idealized Wave−Set Showing the Output Current and Voltage Behavior in a Loss of GND Event.

The idealized wave−set in Figure 29 shows the output behavior in a loss of GND event.

Short Circuit OUT to GND − Current Limitation

In case of an unprotected FET, if the load gets shorted out to GND, there is nothing to limit the current and the power dissipation in the FET (the current eventually be limited by the device trans−conductance, or the current capacity of the supply, or the max capability of the bond wires) which could damage the device. To prevent such a situation of uncontrolled conduction, **onsemi** High−Side devices are equipped with a current limiter logic that limits the maximum current in a device during a short circuit event. The maximum allowed current differs across devices and technologies and can be looked up in the product datasheet. Figure 30 describes the scenario of OUT short circuit to ground− when the switch on the right is closed, the OUT node gets shorted to ground. The device observes a potential difference of V_{BATT} across Drain−Source (ignoring any parasitic line resistance, and the resistance of the short).

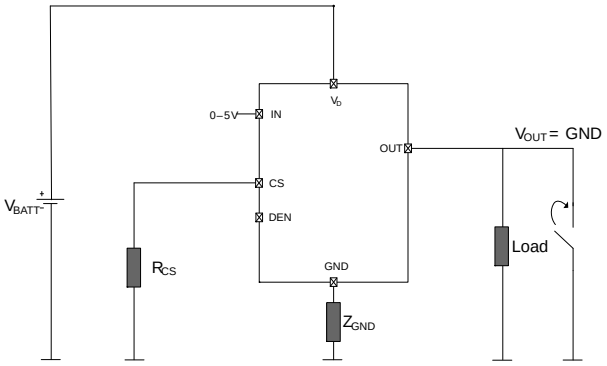

Figure 30. A Short Circuit Event to Ground

Typically, this maximum current, I_{LIM}, is decided based on device's thermal capacity (taking inputs such as size, active silicon area, package etc.), and its intended application. For instance, if the intended application is to drive a bulb load with a high inrush current, the I_{LIM} would have to be set accordingly to ensure the bulb turn−on within the required time. Refer section Bulb Loads for more details on driving bulb loads.

If the short to GND persists, the die temperature would eventually rise even though the current is limited. To preclude high temperature gradients, **onsemi** High−Side FETs incorporate a restart strategy based on differential and absolute temperature sensing (Refer section Temperature/Power Limitation for more information on temperature sensing). The idealized set of waveforms below depicts the exemplary output current behavior in a short circuit event:

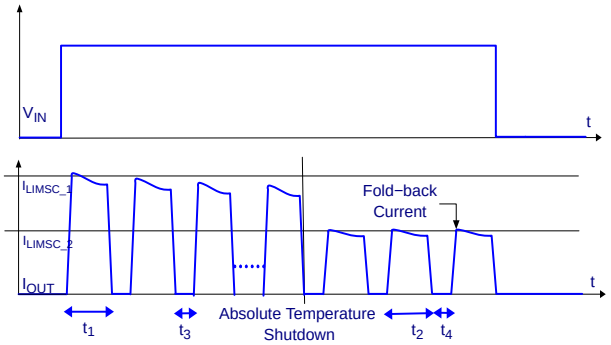

Figure 31. Idealized Wave−Set Describing the Current Limit Behavior with "Fold−Back"

As the device turns on into a short circuit, the current is limited to I_{LIMSC_1} (also referred to as I_{LIM_Hi}). When the differential temperature swing reaches its threshold (Refer Temperature/Power Limitation), the power FET is turned off and turns back on with a hysteresis. The device keeps on toggling on and off with a maximum saturation current of I_{LIMSC_1} until the absolute temperature of the die reaches the maximum limit and thereafter the output current "folds back" to a lower value, I_{LIMSC_2}, to limit the power dissipation, and thereby the temperature rise at high junction temperatures. The turn on times t_1 and t_2 depend on the thresholds for differential and absolute thermal shutdowns respectively (thresholds in terms of absolute and differential temperature limits are defined and specified in the product datasheets); and turn off times t_3 and t_4 depend on their corresponding hysteresis. In addition, the heat sinking and the thermal environment would also impact these time scales. As the device heats up, the circuit controlling the thermal shutdown also observes an increase in temperature which could potentially result in a time lag before these time intervals reach their steady state value.

The current fold−back feature is not universally present across all **onsemi** High Side devices (Refer to specific product datasheets for details). For some devices, a stable RMS current is defined post the absolute thermal shutdown threshold with no fold−back. Such a behavior is presented in Figure 32.

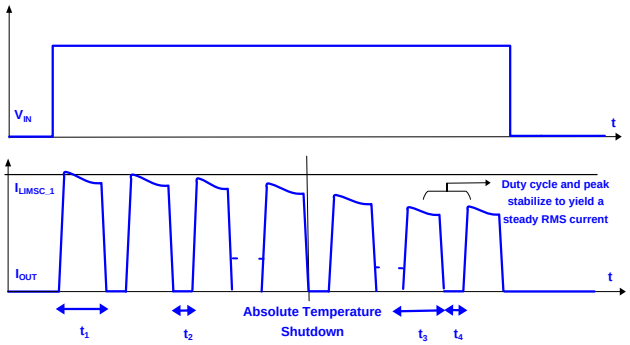

Figure 32. Idealized Wave−Set Describing the Current Limit Behavior Without "Fold−Back"

The current limit circuitry has, in most **onsemi** High−Side FETs, a slightly negative coefficient of variation with temperature to avoid any regenerative increase in current for device safety. Once, the junction temperature reaches the absolute thermal shutdown limit, the peak and the duty cycle of the I_{LIM} pulses stabilizes eventually to yield a steady state RMS current, which is defined in the product datasheet. It should be noted that I_{LIM} is also dependent on the battery voltage, (i.e. the Drain−Source voltage in this case), and is usually specified against a typical battery voltage, or a voltage range. Some devices, like NCV84012A, may also have an I_{LIM} roll off at high Drain−Source voltages to reduce the power dissipation at these high voltages. In case of a "Soft Short" when the resistance in the output conduction path (including the resistance of the short) is high enough such that the output current does not reach the max limit− I_{LIM_SC1}, the thermal protection in the form of Differential and Absolute thermal shutdown and toggling would still be available.

Other than the two current limitation philosophies depicted in Figure 31 and Figure 32, some devices, such as NCV84012A, may incorporate a peak current detect based turn−off in case of a short circuit to GND. The design approach is explained in Figure 33, where the device shuts

off the output stage when the drain current exceeds the internal threshold for current limit, thereby avoiding the higher power dissipation as in case of a linear current limit controlled by thermal shut−down.

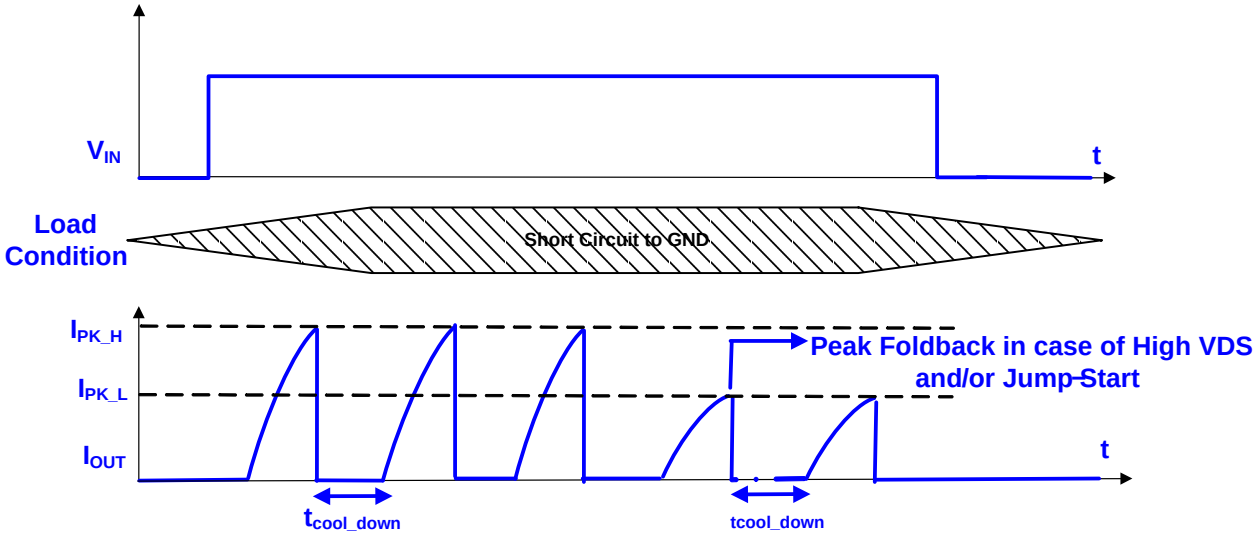

Figure 33. Idealized Wave−Set Describing Peak Detect Based Current Limit

Such a design scheme becomes imperative for devices with high current limits realized on dense technologies where the high power dissipation (in a linear current limit) can be detrimental for the die, and needs to be controlled by a precise peak based turn−off and timer based re−start instead of regulating the current. The “cool−down” timer t_{cool_down} is defined in the control logic based on the safe operating area measurements performed on the technology. Most of these devices also employ a high V_{DS} (as in case of a “hard” short circuit), and/or high V_D (as in case of jump−start) based current limit fold−back. Further, if the absolute or the differential temperature on the die rises over repetitive retries, the longer cool down time enforced by thermal sensors (as explained in the following section) prevails. The majority of devices equipped with this feature also have the capability for trimming the current thresholds and associated timers, offering more design flexibility and a lower device−to−device variability. Refer to product datasheets for specifications on these timer specs, peak detect thresholds and tolerances in the measured peaks.

With reference to relay and fuse replacement solutions, the peak detect based current limit is the preferred choice of design that provides a controlled response in case of a short circuit event and avoids dissipating high power in the loads. On the other hand, applications such as lighting or switching capacitive loads require a steady current over a duration for inrush management. This trade−off is often handled by dialing in peak current thresholds and cool down timers (using trims) pertinent to the load that the device is expected to drive.

Temperature/Power Limitation

Absolute and Differential Temperature Sensing

Fast and accurate temperature sensing serves to protect **onsemi**−High Side FETs in cases of overload and/or high power dissipation events such as Short Circuit OUT to GND. Exceeding device’s thermal capacity is one of the most plausible failure modes in the application, which necessitates employing control elements that could sense and turn off the device when the junction temperature reaches a given threshold. Such a mechanism is termed as Absolute Thermal Shutdown, or simply referred to as TSD (Thermal Shutdown). The typical thermal Shutdown threshold in **onsemi** High− Side FETs is ~175C, unless otherwise specified in the product datasheet. The device turns back on after the die has “cooled down” to a lower temperature. Thermal shutdowns have a hysteresis associated with the turn on to avoid continual thermal toggling around the threshold. There are often many challenges associated with an efficient TSD design− where should the temperature be sensed on the die considering the layout constraints; what should be the optimum tripping point and hysteresis for device shutdown, generating a reference circuitry with minimal variations across temperature etc.

While an absolute thermal shutdown precludes the detrimental damage in case of high power dissipation events, it does not prevent the device from observing temperature gradient during these events, which can

severely affect the lifetime, performance and robustness of the device. For instance, considering a case of a cold bulb inrush, where the ambient temperatures are low and bulb filament needs to be warmed up sufficiently (Refer section Bulb Loads), a high inrush current is conducted through the device which raises the die temperature. In a hypothetical example, where the device ambient temperature is −40 °C and absolute thermal shutdown would occur at ~ 175 °C, the device would observe a thermal gradient of more than 200 °C which may stress the device and significantly reduce the lifetime in case of multiple such events. In some cases these thermal transients result in a thermo−mechanical overstrain which may potentially induce mechanical damages such as die cracks, or delamination. To prevent such a situation, a Differential, or Delta Temperature Sensing and Shutdown (DTSD) mechanism is employed that senses the differential between the max and min die temperatures as shown in Figure 34.

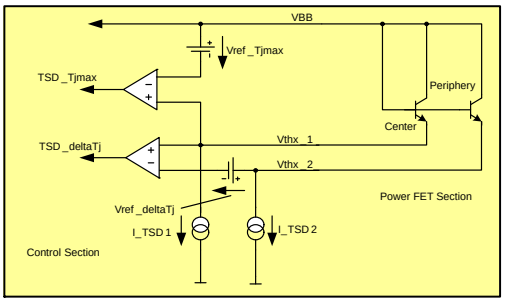

Figure 34. Absolute and Differential Temperature Sensing

Two sense elements are placed− one close to the center of the power FET (that typically observes the max temperature), and the other close to the periphery of the power FET. Since there is a time lag associated with the thermal wave propagation, there is always some difference in the temperature sensed by the two sensors− with the sensor is the centered sensor reading a higher temperature. If the temperature difference exceeds as set threshold, the device is turned off and turns on with a hysteresis. Figure 31 depicts the exemplary electrical equivalent that emulates the thermal behavior described above. The sensed voltages are compared with (thermally) stable references V_{ref_Tjmax} and $V_{ref\_deltaTj}$, and the output is sent to the block that eventually makes the decision to/not to turn off the FET.

Another advantage with this Differential Thermal Toggling is the potential improvement in the Repetitive Short Circuit Performance (RSC). The standard from Automotive Electronics Council− AEC−Q100−012, details the short circuit reliability characterization of smart power devices. In the worst case, device switches an impedance network representative of a short circuit in an automotive environment, and the performance is quantified in grades from A through O (For test setup details and performance classification, refer to AEC−Q100−012). Better performance implies a greater number of pulses survived under the given test and external stimuli conditions. With DTSD, the extent of thermal transient observed in each retry is attenuated and the device can withstand more such short circuit pulses, i.e. an improvement in device lifetime and robustness is observed. The re−try strategy is further explained in the next section. Certain **onsemi** High−side Smart FETs are also equipped with a “back−up” temperature sensor laid out within the control section to protect the device from catastrophic failures.

In the context of SmartFETs with shrunk die sizes, a fast thermal response is indispensable for ensuring the survival off the die in case of transient high power dissipation. The peak current detect is generally designed to meet inrush requirements but may not be sufficient to protect the device under certain conditions. In situations where the short impedance is very small, and a high Drain−Source voltage could occur, the peak current detect may not respond fast enough to the extreme thermal transient experienced by the die. In that case DTSD will take over and ensure that the thermal transient does not exceed the capability of the device. Additionally, a fast absolute thermal shutdown protection can occur when short circuit events happen at elevated temperatures. In this event, thermal sensors are required to safely turn−off the device before the defined peak is attained. This necessitates the sensing and propagation delay to be optimized for a response time on the order of a few tens of microseconds. Applications such as power distribution often operate at higher junction temperatures requiring a higher thermal shutdown threshold in addition to a fast thermal response.

Re−try Strategy

Idealized wave−set in Figure 35 describes the trajectory of the thermal response in a High Side device mapped against the output current in case of Short Circuit OUT to GND. This wave−set essentially adds the temperature curve to the example elucidated in the last section.

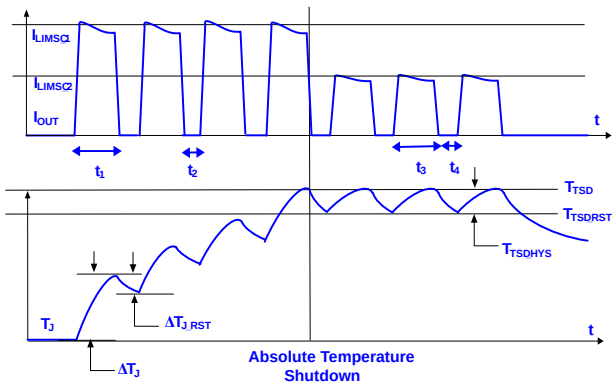

Figure 35. Idealized Waveform Describing the Temperature Trajectory in an OUT Short Circuit to GND Event.

At the beginning of the first pulse, with no power dissipation, the peak junction temperature is equal to the peripheral, or the ambient temperature. As the current rises

to the max limit I_{LIM_SC1}, the temperature rises with a more pronounced increase at the center of the die. When the difference in the two temperatures, ΔT_J, exceeds the defined limit (usually 60 °C in **onsemi** High−Side Devices, unless otherwise specified), the power FET is turned off until the device cools down by ΔT_{J_RST}, and thereafter restarts with another I_{LIM_SC1} pulse. The temperature at the edge of the die increases with each retry cycle as shown in the waveform. Once the peak junction temperature reaches the absolute thermal shutdown limit, T_{TSD}, the device turns on and off with the hysteresis− T_{TSD_HYS}. As explained in section Short Circuit to OUT to GND−Current Limitation, not all **onsemi** High Side FETs have a current fold−back, and the waveforms shown here are just for instance.

The turn on times and hysteresis are chosen with a trade−off between the max temperature transient observed by the die (it is desirable to have a short retry period to avoid large temperature swings), and the ability of a device to turn on a bulb within the given time (long retry periods are desirable to deliver the required bulb inrush with least number of retries).

In contrast to the thermally controlled retry strategy, devices with peak detect current limit employ a fixed timer based retry strategy as discussed before. The number of retries can be indefinite, or internally limited via a counter as in NCV84012A. Figure 36 presents an idealized wave−set in case of a timer−counter based retry strategy. Once a current limit peak is detected, the device is safely turned−off and the counter is incremented. The two parameters− n_{COUNT} and r_{COUNT} are specified in the respective product datasheets. The first n_{COUNT} retries are spaced relatively closer (implying tcool_down < tauto−retry) in time to provide the required inrush for capacitive loads. In case a current limit is still detected after n_{COUNT} retries, the short is then classified as persistent and retries are spaced at longer intervals in time to prevent repetitive over−stress. Once the counter increments to $n_{COUNT}+r_{COUNT}$, the output stage is "latched−off" and disabled until one of the counter reset conditions is met. Figure 36 depicts the enable based counter reset method where the fault counter is reset if device is externally disabled for $t > t_{EN(Rst)}$ (Refer datasheets for timing specification). There may be other reset conditions specific to a device been elaborated in the respective product datasheet. While the figure uses short circuit current limit as an example, the same principle also applies to retries in case of thermal and/or differential thermal shutdown. In devices with timer−counter based retry, the time t_{cool_down} is replaced by (typically longer) thermal hysteresis driven turn−off time. Further, the counter is also multiplexed between the two protection schemes. This implies that the counter value is not over−written as the two protection mechanisms interchangeably control the output stage.

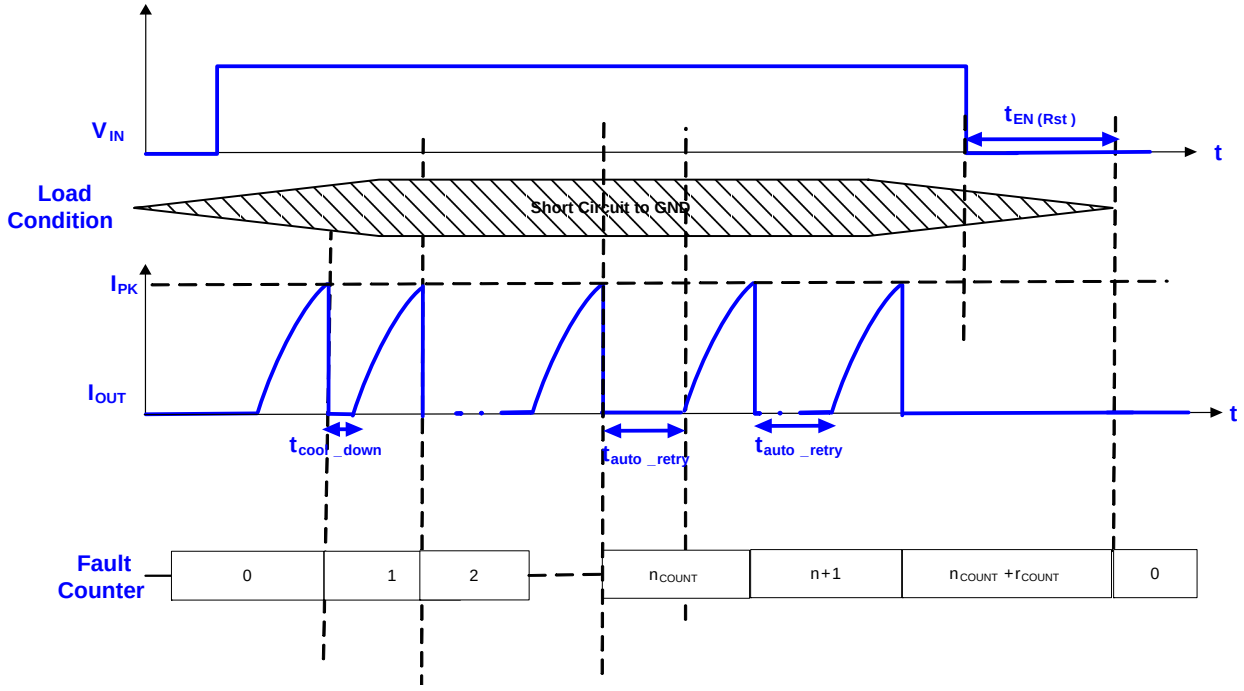

Figure 36. Idealized Wave−Set Describing Timer−Counter based Short Circuit Retry Strategy

Building on the relay and fuse replacement discussion through this note, a short circuit event in such applications does not require the device to retry− successive retrying in short circuit can be catastrophic for the loads connected in the vehicular network through this smart fuse. Having internal trims for the number of retries eases off the design approach for the retry strategy in onsemi SmartFETs where the n_{COUNT} and r_{COUNT} can be trimmed to “1” and “0” respectively in production to cater to a fuse replacement solution.

If the number of retries in a short circuit to GND event is not internally limited, Figure 36, for example, then it is recommended to externally limit the same by the microcontroller in the application. The repetitive toggling of the device impacts the long term reliability and lifetime. While there is no maximum cap for the number of allowed retries, some estimates based on Coffin−Manson analysis specific to the application can be provided on special requests. For certain applications, the load is permanently disabled by the microcontroller if the short persists after a given number of ignition cycles.

APPLICATION INTERFACE AND CONTROL

Pin Interface

The control logic block includes the gate driving (charge pump) circuitry, protection and diagnostic control of the power FET. The input commands and output signals from this block may differ within the family of **onsemi** high side devices (as explained further in this section). The only direct interface input to the power FET is V_D (or the battery connection) and the direct output is OUT, or the source connection to the power FET. Following circuit diagram describes the recommended interface to these pin terminals.

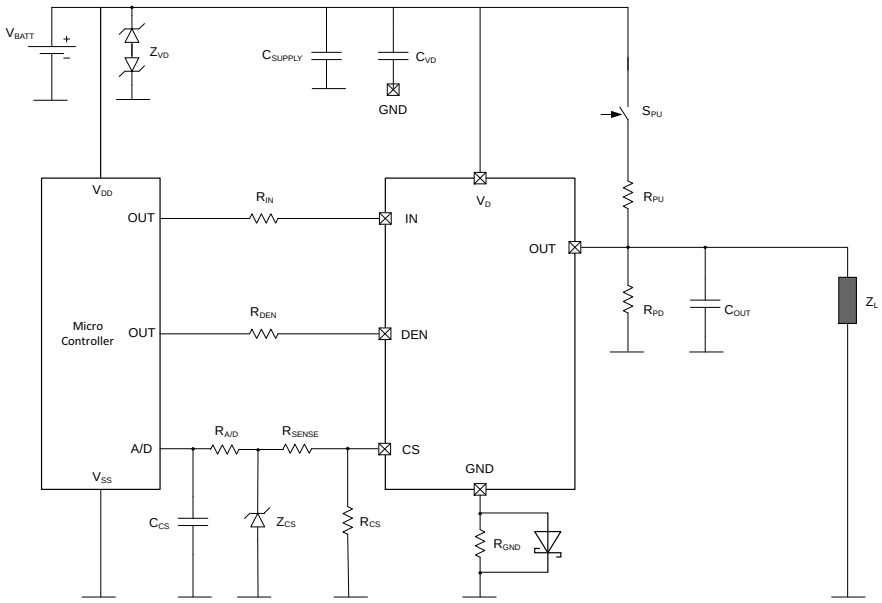

Figure 37. Recommended Pin Interface to onsemi High Side SmartFETs

As in a typical automotive environment, the extremes in the supply voltage V_{BATT} are limited by a stack of zener protection diodes (Z_{VD}), and a capacitive network (C_{SUPPLY}/C_{VD}) filters the transient surges on the supply line. Although **onsemi** high side SmartFETs do offer overvoltage protection (in cases like transient load dump, or jump start), this circuit interface is nevertheless recommended to avoid device operation under abnormal supply voltage conditions. Further, when the voltage spikes at the drain terminal are inflicted because of an inductive flyback consequential to fast output current discharge such as in case of a current limit turn−off, the capacitive network at the drain helps dampen the oscillations and reduce the feed through to the internal digital circuit aiding a stable device operation. The absence of these capacitors may increase the susceptibility of the device to the voltage transients which can also affect the performance such as in−built digital timers. In many cases, the EMI performance of the device is also specified under the assumption that the external drain and output capacitors are connected. For maximum impact, these capacitors are recommended to be placed close to the drain pin on the application PCB, as compared to the zener voltage suppressors, which are typically placed close to the alternator. The parasitic cable impedance in the V_D connection to the supply should be minimized in the application as it reduces the available rail−to−rail voltage for the device operation. This could especially be challenging under low battery voltage conditions such as cold cranking, making it difficult for the device to operate with nominal protection and diagnostic capabilities. Section Typical Supply Voltage Specs mentions the typical operating voltage ranges. Further, in case of sufficient potential drop between V_{BATT} and V_D, an output short to V_{BATT} can create an inverse current scenario which could be highly stressful for the device.

The resistors R_{IN} (at the input pin) and R_{DEN} (at diagnostic enable pin) are interfaced between the microcontroller and the high side device. It should be noted that different devices within the **onsemi** high side SmartFET family may have different topologies for enabling/disabling the diagnostic output (Refer CS Enable/Disable Logic) through a digital signal, and the term DEN has been used for generic purposes here. Further, based on the specific device topology, the input command could also be active−high or active−low. Unless otherwise mentioned, an active high digital command will be considered through this document while referring to the input signal. The resistors in series with these digital inputs protect the microcontroller output in case of an over−voltage event and also limit the current through the internal ESD structures, Z_{ESD} to these pins (Refer Figure 26) in case of a reverse battery operation. In addition, these resistors also prevent the high−side device

from finding any parasitic grounds (through microcontroller) in case of a loss of ground situation. While these series resistors do offer protection as described above, it is important to have an understanding of how to size these resistors. The sizing implications are mainly driven by the microcontroller drive current capabilities, and the required input current and voltage to turn on and turn off the device input. A bigger resistor would imply a bigger potential drop, and consequently the microcontroller should output a higher voltage to ensure sufficient turn−on voltage for the device input stage. Likewise, while reducing the resistor value, the output voltage level should guarantee a proper device turn−off.

$$V_{OUT\_MICRO} = V_{RIN} + V_{IN} + V_{GND} \quad \text{(eq. 3)}$$

where V_{OUT_MICRO} is the output voltage from the microcontroller, V_{RIN} is the potential drop across the series resistor $R_{IN,}$ V_{IN} is the input voltage required at the input stage of the high side device (for turn on/turn off) and V_{GND} is the potential drop across the ground impedance. A similar equation applies for the DEN pin as well.

In some applications, protection clamps are also placed at the device input pins (specifically where the output stage of the microcontroller can observe surges or where the protection structures within the microcontroller are not present). For specific recommended values for these resistors, refer to product datasheets.

The network interfaced to the current sense pin consists of a sense resistor R_{CS}, a current limiting (through the zener clamp) resistor R_{SENSE}, a zener clamp Z_{CS} to limit the voltage swing at CS output (the voltage at CS output can rise all the way up to V_D) and an RC noise filter for the microcontroller's input A/D stage. The analog current sense output as well as the fault state output current from the CS pin is converted into a voltage across R_{CS} and subsequently digitized by the micro's A/D stage. For further details on the selection of R_{CS} and the behavior of CS output, refer to section CS Pin Interface and Sensing the Current.

The GND pin is recommended to be connected to a parallel combination of a diode D_{GND} and a resistor R_{GND} (in some cases, only a resistor can suffice as the GND network depending on the value of resistor chosen). The GND network protects the device in case of an overvoltage event and also limits the current in case of a reverse battery connection. The details of the GND circuit operation and the suggested values for the diode and resistor are mentioned in section Recommended GND Circuit. A loss of ground situation is also depicted in section Loss of Ground.

The output terminal is connected to the desired application load Z_L with an output capacitor, C_{OUT}, to protect the load from transient output voltage swings. The value for this capacitance should be chosen not to interfere with the typical switching frequencies for a given device (generally recommended in the product datasheets). Typical automotive loads and the corresponding output behavior are detailed in section Application Environment and Loads. The peripheral network at the OUT pin consisting of the switch S_{PU} and resistor R_{PU} serve for off state open load diagnostics. The resistor R_{PU} needs to be sized in accordance with the leakage resistance for the specific device, and the switch eliminates the power dissipation (or the leakage current) through this resistor when off state open load diagnostics is not required. For details on the resistor selection criteria, see section Open Load Diagnostics. The pull down resistor, R_{PD} is employed to diagnose a short circuit to battery event and differentiates this fault from off state open load through output voltage read−out (Refer section Short Circuit to Battery). Specific recommended values for these resistors can be referred to in the product datasheets.

Many SmartFET's have "No Connect (NC)" pins, often present to ensure package compatibility across family of devices (such as single and dual channels). While in most cases these pins are not connected internally and do not affect performance of the device, some devices utilize these pins especially for digital trim programming in production and design mode analysis. In these devices, it is always recommended to short these pins to GND through a protection resistor to avoid any inadvertent operation. Specific datasheets should be referred to for recommended connections to NC pins.

Input Control and Hysteresis

The application microcontroller commands the input (and the diagnosis enable/disable pin) with digital (standard logic level) signals which then drive the output FET and also control the diagnosis through current sense. The block diagram in Figure 38 depicts the control and conditioning of this digital command inside the device.

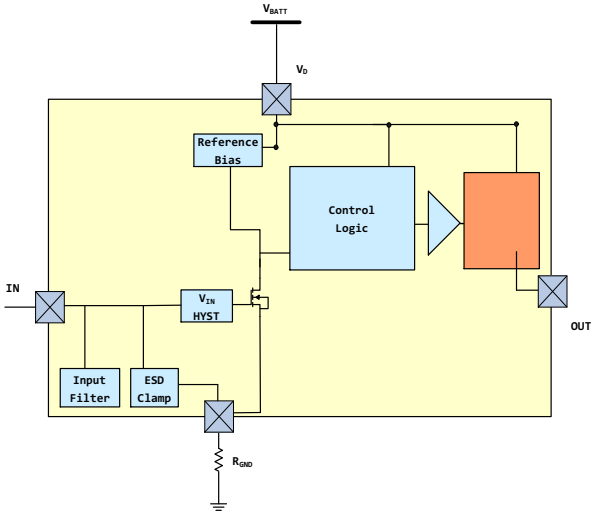

Figure 38. Block Diagram Showing Input Control and Hysteresis

The first stage in signal conditioning is to filter any transient noise associated with microcontroller's output with a low pass filter stage. An integrated ESD clamp zener (referenced to the ground terminal) limits the voltage swings observed at the input terminal. In case of an overvoltage

event, the digital inputs are clamped to a diode drop less than the GND potential, while in a reverse battery situation these zeners break down and the current is limited through the series gate resistors (Refer sections Over−Voltage Protection and Reverse Battery Protection for details on overvoltage behavior and reverse battery protection respectively). A hysteresis circuit (comprising of a MOSFET with an adjustable potential divider stage at its gate) conditions the input command and drives a switch as shown in Figure 39 (the hysteresis circuit is included in the block marked as V_{IN_HYST}). Hysteresis prevents the device from repetitive switching most likely in case of a noisy input signal (some low frequency noise remains unfiltered after the input filter stage).

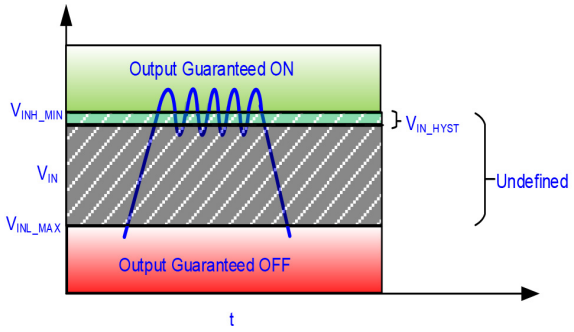

Figure 39. Input Signal Level and Hysteresis

As explained in Figure 39, two primary logic levels are defined for the input signal. V_{INL_MAX} is the maximum low level voltage to ensure output FET turn off; and V_{INH_MIN} is the minimum high level voltage to ensure output FET turn on. These levels are mentioned in the respective product datasheets. Any input level in between these two creates an undefined state and the output FET could either be on or off. Such a situation should be avoided− in other words, an input signal level between V_{INL_MAX} and V_{INH_MIN} should be avoided by application microcontroller. Figure 39 also explains the concept of input hysteresis. In case of input signal noise, an absence of hysteresis can cause the transistor to switch on and off repetitively as it crosses the threshold required for turn on. Adding hysteresis ensures that the transistor stays on until the falling transition of the input signal crosses over the hysteresis threshold thereby preventing the unnecessary switching and associated switching energy losses. It should be noted that the hysteresis threshold defined in Figure 39 (V_{IN_HYST}) is only typical and could vary within the window defined by two logic levels. While the output FET should turn off below the hysteresis threshold on a falling input transition, it is "guaranteed" to be turned off only below V_{INL_MAX}. Therefore, it is imperative to reiterate that all signal levels between V_{INL_MAX} and V_{INH_MIN} should be avoided in the application. For typical V_{IN_HYST} levels, refer to product datasheets.

After the hysteresis block, a switch controls the command fed into the control logic block which then drives the charge pump to turn on/off the output stage. In addition, this signal is also fed to the current sensing control for diagnosis. A similar circuit block as in Figure 38 is employed for the diagnostic enable/disable (DEN) signal as well.

The circuit interface in Figure 37 depicts a single channel device. In case of a multi−channel device, the input control circuitry is duplicated over all channels within the device. The recommended peripheral circuit stays same for inputs and outputs across channels. The analog current sense output is generally shared by all the channels and a digital channel select input (see product datasheets of multichannel devices for details) multiplexes the sense outputs of different channels into a single CS output. The microcontroller interface to this digital channel select input and the controlling circuit block (inside the device) is identical to other digital inputs.

SWITCHING CHARACTERISTICS

Optimal switching performance is the primary operational requirement from any MOSFET. This includes achieving the desired switching speed with sufficient drive capabilities for the desired load while minimizing the losses during switching. **onsemi** High Side SmartFETs are designed to cater to switching requirements over a range and types of loads. This section deliberates the behavior of a High Side SmartFET while switching typical application loads− resistive, inductive and bulb (capacitive) loads.

Resistive Switching

Resistive loads are the most typical of an application environment; and with the increasing use of LEDS for automotive lighting solutions (both interior and exterior lighting− refer section Resistive Loads), the thrust for resistive loads is compounding. While resistive loads do not associate with the asymmetrical polarity challenges (as in inductive loads, relays etc.), they often require higher switching speeds with dynamic current sensing and diagnostics− for instance, PWM of an LED load. Further, if the same device is used to switch alternatively between a high wattage bulb load and a string of LEDs, the transition from one load to another should be smooth while complementing the high power drive capability (for a bulb) with a precision current sensing required for an LED load.

The idealized wave−set in Figure 40 depicts the output behavior under resistive switching:

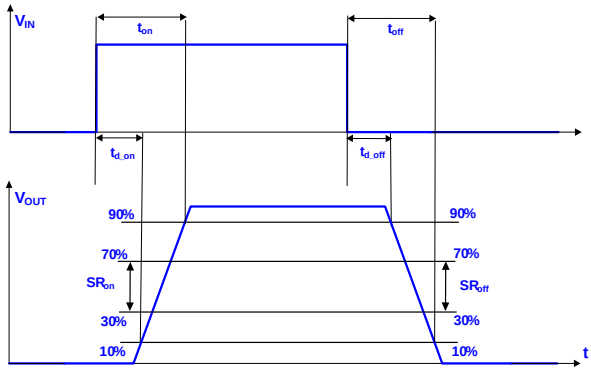

Figure 40. Input and Output Transitions During Resistive Switching

The time intervals and the corresponding timing markers on the voltage waveform trajectories have been indicated in Figure 40. The definitions are as follows (unless otherwise mentioned in the datasheet):

t_{d_on}: the delay time from the rising edge of input command to 10% of output voltage

t_{on}: total turn on time from rising edge of the input command to 90% of output voltage

t_{d_off}: the delay time from the falling edge of input command to 90% of output voltage

t_{off}: total turn off time from falling edge of the input command to 10% of output voltage

SR_{on}: Slew rate from 30% to 70% of output voltage during turn on

SR_{off}: Slew rate from 70% to 30% of output voltage during turn off

The relative difference between turn on and turn off slew rates is referred to as slew rate matching. Certain **onsemi** High Side Devices, for instance, NCV84012A, NCV84008A etc. have a sleep mode feature incorporated (typically when both input command and diagnostic control have been deactivated for a given time) to reduce the leakage levels. The turn on times in cases where the device is activated from a sleep mode may differ from the usual turn on times. Refer to respective product datasheets for specifications on switching time intervals with sleep mode.

The turn on and turn off delays are mainly associated with enabling and disabling the charge pump, and the slewing is generally controlled with an active circuit at the gate of the power FET. These timing parameters are specified against a set of conditions such as load resistance, battery voltage, ambient temperature etc. The conditions and the timing specifications can be looked up in the specific product datasheet. As mentioned before, while switching loads, the current sensing and diagnostic delays need to be considered (See Figure 56 for current sense timing parameters). The PWM frequency and duty cycle should be set such that the device is able to output the proportional sense current and report fault, if any, with each cycle of the input command. **onsemi**'s family of high side SmartFETs meets the switching speed requirements for most automotive loads.

The switching energy losses primarily depend on the charging and discharging of input (C_{GS}), transfer (C_{GD}) and output (C_{DS}) capacitances. These capacitances are a contribution of the parasitic device effects and depend mainly on the geometrical feature size. A transistor with a higher active Si area may have a lower $R_{DS(ON)}$ (and therefore lower conduction losses) but the switching losses could be significant because of increased device capacitances. All these factors are accounted for in during the design and layout stages to achieve the optimal performance. In addition, these losses also depend on the application frequency and should be considered by the OEM while defining a requirement specification.

While a higher switching speed helps in reducing switching losses and also satisfies the PWM requirements, it is not necessarily always desirable in the application because of a possibility of infringing with EMI/EMC requirements. For this reason, the speed of the device is controlled and sometimes even compromised to ensure compliance with the required EMI performance. This slew rate control is better conceptualized in Figure 41.

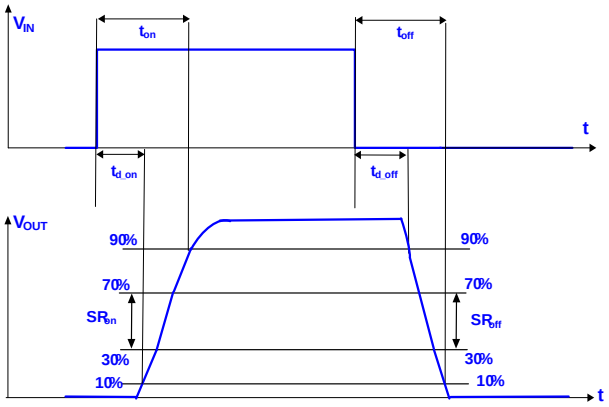

Figure 41. Input and Output Transitions With Slew Rate Control During Resistive Switching

As depicted in the waveforms above, the output FET turns on relatively slowly as the charge pump is enabled. This is followed by a fast gate charge ramp up, and as the output reaches its steady state level (i.e. the transistor is fully on), charge pump regulates and pulls back on the gate charge to avoid any overshoots. The regulation mechanism may or may not be present depending on the specific control technology (Refer section Charge Pump−Principle of Operation). At turn−off, the gate charge is removed rapidly as the charge pump is disabled in the beginning which is

followed by a slow controlled discharge. These different regions of fast or steady gate charge (and discharge) render design flexibility in controlling the EMI performance while achieving the desired switching speed. It should be noted that the slope transitions in Figure 41 have been indicated rather conspicuously to conceptualize the mechanism. In practice, output voltage transitions are smooth and do not involve any kinks or dips.

In addition to the EMI implications cited above, some devices exhibit reduced slew rates (turn on slew in particular), at loads heavier than nominal. These loads are generally observed in the application during short circuit events− could be a “soft short” or “hard short” depending on the short impedance. Slowing down the turn on trajectory provides an improved control over the current limit profile that allows to reduce and (in some cases) even eliminate oscillations while attempting to regulate the output stage at high current levels. The switching speed (and consequently switching energy) and slew rate matching at short circuit loads, therefore, are often traded−off for a stable operation with no overshoots/undershoots in current limit.

In fuse replacement applications, externally programmable slew rates are seldom required to differentiate the turn on (after cranking) from a short circuit event. Reducing the slew rate externally at power on provides the inrush required to energize the capacitive loads downstream. A fast turn on slew, on the other hand, leads to the output current ramped up quickly to the short circuit threshold which permanently latches off the output stage. While onsemi High Side SmartFETs currently do not offer an externally programmable slew rate feature, the slew control at heavy loads discussed above is a step in the direction of targeting fuse replacement solutions. Since a fuse is rarely required to switch (periodically) in the application, the switching speed and PWM requirements for a fuse replacement SmartFET are not as stringent as that for other conventional applications.

Inductive Switching

Relays and inductive loads are integral to the operation of most automotive applications. Inductive loads do not switch with the same polarity on the output terminal and the inverse voltage swing at the output terminal needs to be limited during the inductive flyback event. This is typically done using the Drain−Gate over−voltage protection diodes, Z_{CL}. Figure 42 is a block diagram representation of an inductive switching scenario.

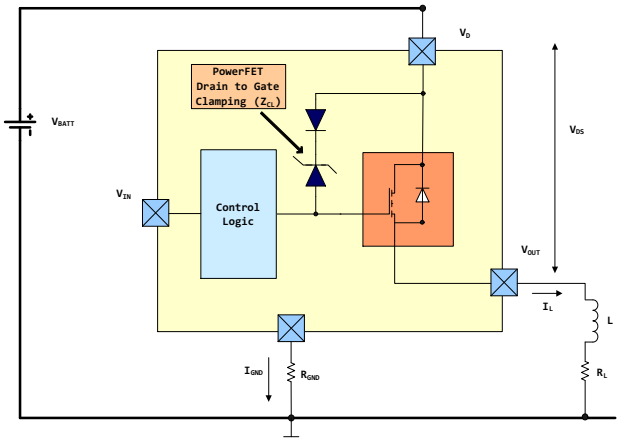

Figure 42. Inductive Switching Block Diagram

When the input command is turned High, the inductor gets charged to a peak current determined by the magnitude of inductance, drain potential V_D, line resistance, R_L and the “dwell time” (time for which the device is turned on). The output potential at this time is $V_D−V_{DSON}$. Once the input command is turned Low, the output current starts to decay, and a voltage is developed across the inductor that opposes this current decay. Since the discharge voltage and current in an inductor bear opposing polarities, the output terminal observes a negative swing. In the absence of overvoltage protection clamp diodes, this swing will be limited by the breakdown (or avalanche) of the body diode. Such a situation can be stressful for the device as a confined area on the die (in the vicinity of the body diode) will conduct a high current density and can lead to the generation of localized “hot−spots” on the die. Further, avalanching the body diode each time during inductive switching may compromise its long term reliability. To avoid this, an active Gate−Source circuit is enabled at the time of device turn off, and controls the conduction path comprising of Drain−Gate clamp diodes, Gate−Source impedance and the inductive load. When the voltage across the Gate−Source impedance reaches the required input threshold of the device, the output FET turns on and conducts the current discharged by the inductor with the return path through the battery and supply ground. This mechanism is termed as “active clamping” and the current density in this case is distributed across the entire active area of the power FET which prevents the formation of any local current constriction channels. In applications where the output voltage is sensed by the microcontroller, active clamping limits the magnitude of output voltage observed by micro, thereby protecting its I/O interface. If the battery during an inductive flyback event is disconnected (or the battery connection is lost), the return path in an inductive discharge would consist of the protection diodes for the control logic circuit and the device’s ground impedance network. This circuit path is not designed to conduct such high power events and may get damaged. Such a case can be avoided by employing free−wheeling diodes for providing a return path for inductive discharge.

The idealized wave−set in Figure 43 describes the output current and voltage transitions while switching an inductor.

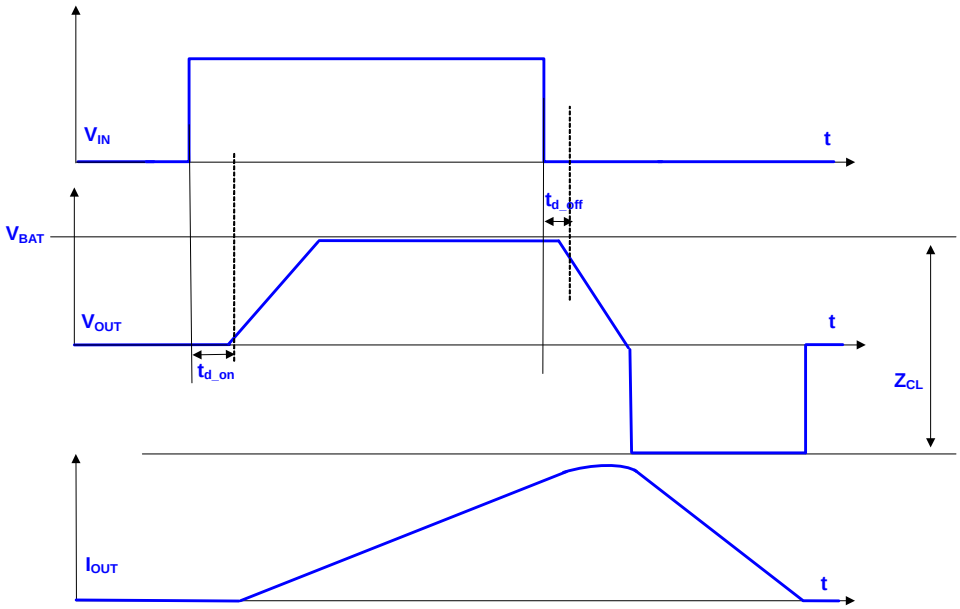

Figure 43. Input and Output Transitions During Inductive Switching

The waveforms above neglect any parasitic line resistance as well as the internal resistance of the inductive load. In case of a significant series resistance, the output current trajectories would not be linear and exhibit an exponential curvature marked by a time constant, $\tau = L/R$. It should be noted that the output voltage attained in the reverse direction is a function of battery voltage:

$$V_{OUT} = V_D - V_{ZCL} \quad \text{(eq. 4)}$$

Where V_{ZCL} is the breakdown voltage of the overvoltage protection clamp diodes.

The inductive discharge capability of a device is usually quantified by the metric− SCIS (Self Clamped Inductive Switching) energy. In an ideal inductive discharge event, considering no losses, the energy can be calculated as:

$$E = \frac{1}{2} \cdot L \cdot I_{pk}^{\ 2} \quad \text{(eq. 5)}$$

Where I_{pk} is the peak current inductor is charged to. In the application, however, the discharge is not ideal, and the power supply stays connected all through the charge and discharge cycles. This reduces the available voltage to discharge the inductor, and consequently increases the discharge or the avalanche time, t_{av}. This effect is conceptualized in an “effective inductance” discharged where

$$L_{eff} = L \cdot \left| \frac{V_{ZCL}}{V_D - V_{ZCL}} \right| \quad \text{(eq. 6)}$$

This effective inductance is greater than the physical inductance L, and the energy discharged is calculated as:

$$E = \frac{1}{2} \cdot L \cdot I_{pk}^{\ 2} \cdot \left| \frac{V_{ZCL}}{V_D - V_{ZCL}} \right| \quad \text{(eq. 7)}$$

The calculations and equations above do not include the effect of series line resistance. Taking that into account, the avalanche time and the inductive discharge energy are stated as follows.

$$\tau_{av} = \left| \frac{L}{R} \cdot In\left(1 - \frac{I_{pk} \cdot R}{V_D - V_{ZCL}}\right) \right| \quad \text{(eq. 8)}$$

$$E = V_{CL} \cdot \frac{L}{R_L^{\ 2}} \cdot \left(V_D + \left(V_D - V_{ZCL}\right) \cdot In\left(1 - \frac{I_{pk} \cdot R}{V_D - V_{ZCL}}\right) \right) \quad \text{(eq. 9)}$$

The energy ratings are specified in the product datasheets for a single pulse inductive discharge as well as over a Repetitive Clamp (RCL) event. An RCL test subjects the device to repetitive clamp cycles while discharging an inductive load. In the context of **onsemi** High Side SmartFETs, the switching frequency is sufficiently low to ensure that the die “cools down” to ambient temperature at the beginning of each charging cycle (Refer Section Understanding the Thermal Network for understanding the impact of inductive switching on die temperature). The RCL rating, in terms of max current switched at a given inductance and ambient temperature, is defined over 1 million cycles of operation. Intuitively, this rating is lower than the Single Pulse Inductive Switching rating. These ratings are typically plotted over a range of inductors and temperatures to help the customers select the inductive load

and the corresponding drive current accordingly (The energy dissipated across the device at a given inductance should not be more than the rated energy per the datasheet).

Bulb Switching

Bulbs in principle emulate the transient output characteristics of a capacitive network with the current being maximum at the time of turn on gradually decreasing towards the steady state current determined by the resistance at full turn on. The high side device should be able to support the required inrush profile for bulb turn−on. A change in the filament resistance (through the turn on period) gives rise to a non−linear impedance profile. Section Bulb Loads describes the electrical characteristics of typical bulb loads− for instance, wattage, inrush etc. and also suggests the suitable **onsemi** High Side SmartFET to switch specific bulb loads. The phenomenon of bulb inrush and the strategies for handling inrush− with, or without auto retries are also explained in section Bulb Loads.

The dynamic switching behavior and operating mode of a high side FET during a bulb control is quite different from that in case of LED or inductive loads. Although bulbs have same output polarity (at turn on and turn off) similar to a resistive load, the retries during the inrush phase have the device working in linear mode with the maximum current limited to I_{LIM}. With the last retry, the device transitions from linear to $R_{DS(ON)}$ mode as the current approaches the nominal current. This transition should be smooth and avoid any jitters/abrupt output level or current changes to avoid undesired flickering of the bulb post inrush. The situation is depicted in the idealized wave−set on the right showing the output current transitions during a bulb turn on.

At t = 0, when the device is turned on, the current gets limited to I_{LIM} and the device “regulates” as it turns on and off with differential thermal shutdown threshold and hysteresis (refer section Temperature/Power Limitation) for the subsequent retries. The gate of the output FET is controlled by the I_{LIM} control circuit that overrides the charge pump. The last couple of retries have been highlighted in red, and this is where the device stops regulating and charge pump takes over the gate control. The I_{LIM} control circuit is expected to switch in and out without associating any crosstalk with the charge pump operation.

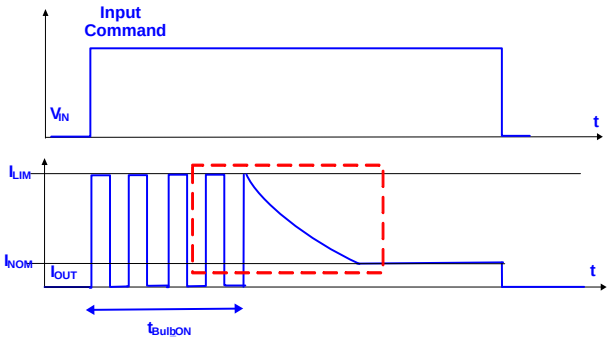

Figure 44. Output Current Transitions in Re−Tries During Bulb Inrush

While differential thermal shutdown reduces the transient thermal stresses on the device, it increases the time required to *sufficiently* (typically when the load current decays to half the inrush) turn on a bulb with re−tries. In devices where the short circuit is primarily controlled by current limit peak detect methodology (Refer Section *Short Circuit OUT to GND − Current Limitation*), the bulb turn on times may further be impacted to ensure safe operation of the SmartFET. The peak current threshold and cool down times are therefore designed to balance the trade off between recommended bulb inrush requirements while guaranteeing a safe operation of the device. The high side device should be selected appropriately such that it is able to turn on the bulb in the required upper limit for the turn on time (refer section Bulb Loads).

Since the time required to turn on the bulb will also depend on the line parasitic impedance which may change across applications, it becomes difficult to recommend a SmartFET specific to a bulb. To circumvent this challenge, turn−on times are measured in a standard circuit configuration per Figure 45. The voltage at the drain of the SmartFET is actively regulated at the desired reference level by a high precision fast op−amp driving the high side referenced regulator. The parasitic resistance is minimized by using thick and short cables for drain and output connections. The active circuit eliminates any drop in the drain voltage as observed by the SmartFET as it is conducting high levels of inrush current. The schematic does not describe connections to other terminals such as CS, DEN, GND etc. These terminals need to be interfaced per the standard application circuit and will not have any perceptible impact on the inrush timing. Recommendations are always made per the worst case scenario where the bulb observes an ambient temperature of −40°C and the DUT (Device Under Test) is placed at room temperature ambient. It should be noted that this measurement circuit is employed only to allow for a standardized bulb recommendation across the family of devices, and is not the required circuit in the actual application. Refer Section Application Interface and Control for details on recommended application circuit.

Another consideration while switching bulbs is the possibility of an intermittent loss of or dip in the supply voltage. The high side switch should be able to “react” fast post the battery voltage reaches the nominal value, and source in the required inrush profile with minimal delay to ensure bulb turn on in desired time.

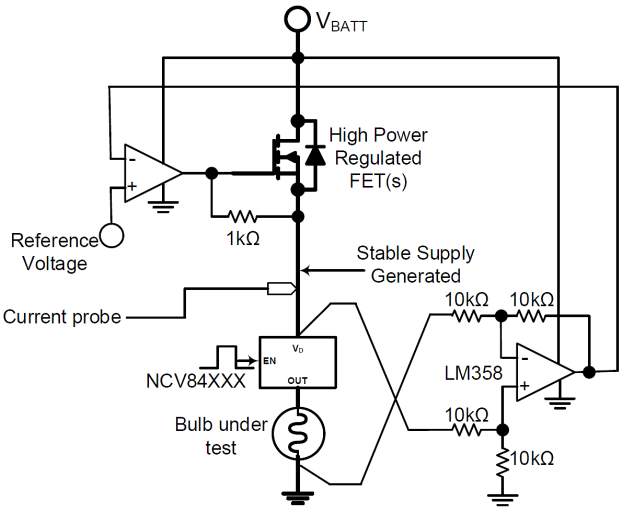

Figure 45. Bulb Inrush Timing Measurement Circuit

CURRENT SENSE AND DIAGNOSTICS

onsemi High−Side Smart FETs are equipped with an analog current sense (CS) output. This output serves two objectives− a) Depicts the level of output current flowing through the power MOS and b) Indicates an existing fault condition, if any (For details on fault conditions, refer to section Current Sense Behavior in Normal and Fault States).

Operational Methodology

The current in the power FET is sensed through a “Sense FET” integrated within the device. This Sense FET is usually a small mirrored branch−out from the power FET, or the DMOS, with the drain and gate terminals tied to those of the DMOS. Figure 46 is a block diagram depicting the current sense mechanism, and Figure 47 describes the device principle (using a trench−FET as an example):

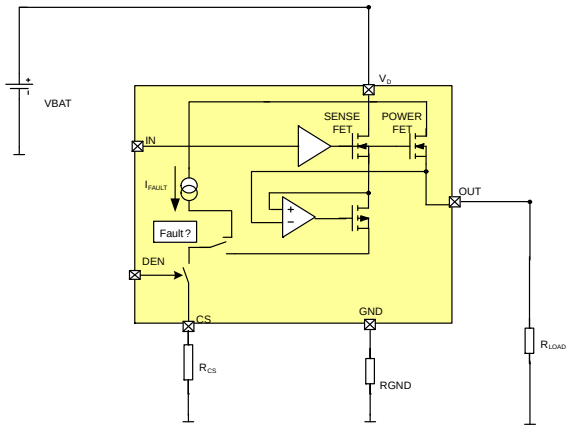

Figure 46. Block Diagram Depicting the Current Sensing Mechanism

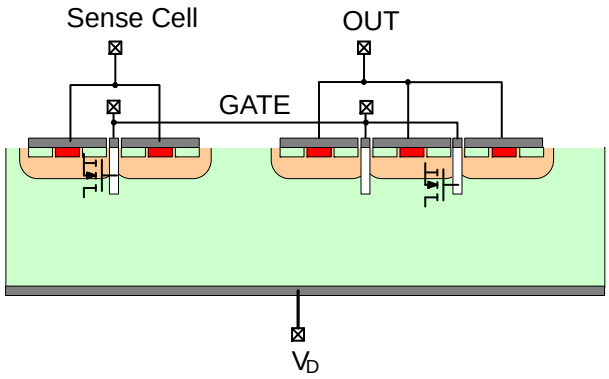

Figure 47. Current Sense − Device Operating Principle

As stated above, the power and sense FETs have common gate and drain terminals; the major challenge in a current sense design is minimizing the difference in the source potentials. In theory, a true current mirror operates in current regulation mode with minimal dependence on Drain−Source voltage (such that the sensed current is solely dependent on the relative aspect ratios of the two FETs). However, for the applications under consideration here, the power FET is required to be turned fully on as a switch, with a strong dependence of current on the Drain−Source voltage. Thus, any offset in the source potentials will deviate the sensed current (or the Sense Ratio), from its expected value. The block diagram includes a high gain op−amp that forces the two sources at the same potential. In an ideal scenario, when there is no offset between the source potentials, the ratio of the currents in the Power and Sense FETs is directly calculated from the geometrical (Active Area) ratios (represented by the constants $K_{1/2}$ in Eq. 11), given the two FETs have perfectly matched electrical, physical and structural characteristics. However, such a design is hard to achieve in practice. The offsets in the analog circuitry (primarily, the op−amp), and the transistor mismatches associate an error factor with the absolute sense ratio, which becomes more pronounced at light loads (Refer section

Current Sense Accuracy Improvement at Light Loads and Current Sense Calibration)

$$I_{LOAD} = I_{OUT} = K_1 \cdot (V_{OV1})^2 \cdot (1 + \alpha V_{DS1})$$

$$I_{SENSE} = K_2 \cdot (V_{OV2})^2 \cdot (1 + \alpha V_{DS2}) \quad \text{(eq. 10)}$$

$$SR = \frac{I_{LOAD}}{I_{SENSE}}$$

K_X is the constant accounting for device's physical dimensions,

V_{OVX} is the overdrive voltage

α is the channel length modulation coefficient

V_{DSX} is the drain−source voltage drop, and

SR is the sense ratio.

As shown in Figure 46, the current flowing through the Sense FET is measured as the voltage across the sense resistor, R_{CS}. The load current is then estimated using the sense ratios specified in the product datasheets under different conditions. In case a fault condition exists, the fault−state current source over−rides and CS pin reads a fault−state voltage. The fault state current, (and the corresponding voltage measured across R_{CS}) is typically higher than the maximum sensed current under normal operation, to distinguish the fault condition from no−fault condition. Both the normal state and fault state sense currents exhibit a dependence on temperature (with a slightly negative coefficient of variation) and battery voltage. As the battery voltage droops, the current source, driven by the op−amp output, runs out of the required "head−room" and fails to regulate eventually. This results in the reduction of sense current. The next section describes the selection criteria for the sense resistor to ensure the desired behavior from the CS output. The Diagnostic Enable (DEN) pin enables/disables the current sense output and could be either an active high or active low logic input depending on the specific device (Refer section CS Enable/Disable Logic). In addition to an efficient circuit design, a reliable current sensing also requires an optimal (and stable) layout. Highlighting (in red) the current sensing section from Figure 12 in the die image on the right, it is desirable to have the sense FET relatively centered within the power FET and any constrained geometrical features should be avoided for a uniform current density.

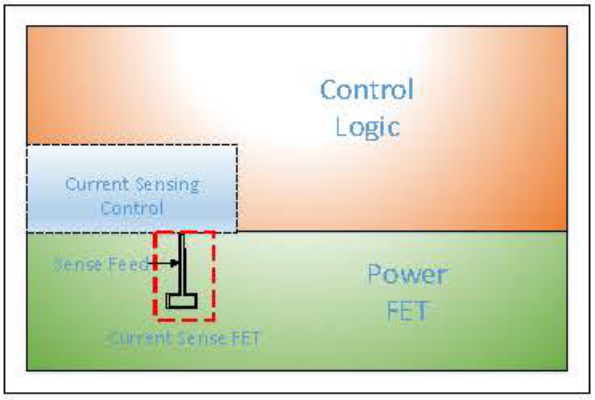

Figure 48. Exemplary Layout Highlighting Current Sense Block And Sense Feed

The dashed rectangle in red encloses the "Sense Feed" that bridges the sense transistor to the control logic section. Any parasitic conduction paths between the two FETs (Sense and Power) should be taken into consideration during the design stage. Intuitively, a device with higher sense ratio is difficult to layout and fabricate than that with a small sense ratio because of smaller geometries associated with the Sense FET.

CS Pin Interface and Sensing the Current

This section describes the current sense pin interface to the microcontroller. Figure 49 below focusses on the current sense block only from Figure 37. The resistance, R_{CS}, senses the current output from the CS pin. The voltage developed across R_{CS} scales linearly with the magnitude of R_{CS}, given a constant sense current is sourced by the CS pin. This assumption is valid, only until certain values of R_{CS}. For really high sense resistors (typically > 10 kΩ), the internal current source fails to regulate (because of headroom limitations, as mentioned before) and the current coming out of the CS pin decreases, thus saturating the voltage across R_{CS}. Such a behavior is plotted in Figure 50. The voltage, V_{SENSE}, across R_{CS}, increases linearly until $V_{(SENSE)\ SAT}$ and then saturates.

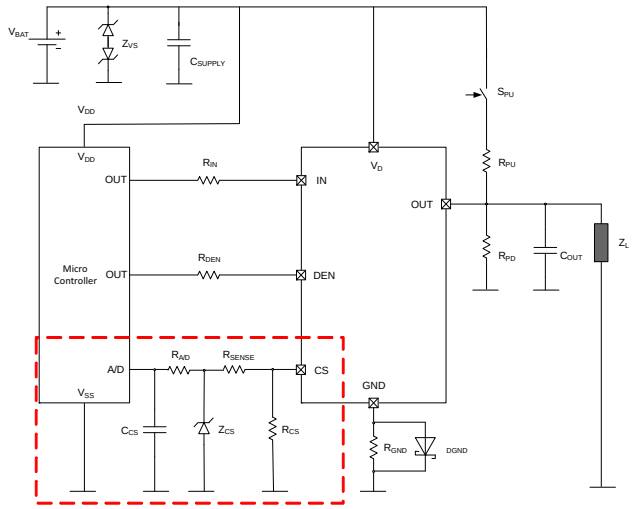

Figure 49. Microcontroller Interface to CS Pin

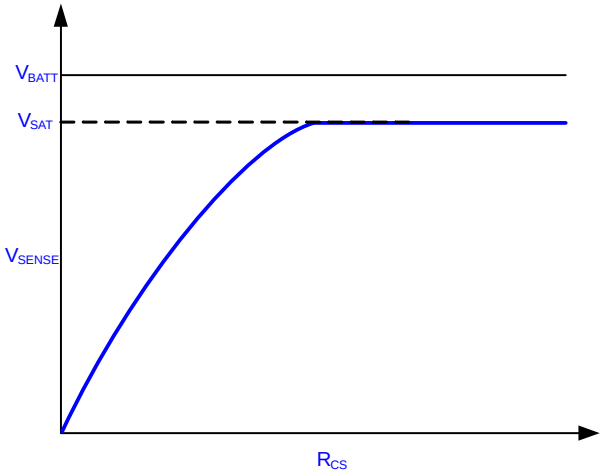

Figure 50. Variation of Sense Voltage vs R_{CS}

The $V_{(SENSE)\,SAT}$ level, though typically close to V_{BATT}, may change across devices and technologies, and specific product datasheets should be referred to for sense saturation voltages. As the sense current decreases, the sense ratio increases and the error factor associated with the estimation of load current becomes more pronounced, which is undesirable. The discussion so far focused on the operation in a normal, or non−fault state. If a fault condition exists, the fault state current source (Refer Figure 46) is active and forces current out of the CS pin. Depending on the specific device design, V_{SENSE} may rise all the way up to V_{BATT} (less a marginal drop across the internal circuit elements) for large R_{CS} values, as in NCV84160, for example; or have a fixed saturation point below V_{BATT}. To summarize, too large of a sense resistor, may saturate the sense voltage creating an error in the output sense current (and therefore, the estimated load current). Also, it is difficult to differentiate (with sufficient confidence) between the fault and no−fault state V_{SENSE} for high values of R_{CS}. In case too low of a value is chosen for the sense resistor, the sensed voltage may be too small to be sampled by the A/D of the microcontroller. Additionally, high precision small sense resistors can be expensive and may raise the system cost. Considering these implications, the sense resistor should be chosen optimally−typically a value in the range of 1 kΩ ~ 5 kΩ is recommended. The product datasheets should be referred to for any specific recommendations.

In addition to the voltage headroom limitation, the sense ratio accuracy also depends on the drive current capability of the analog circuitry, particularly the current source feeding the sense FET (Referring Figure 51, the PMOS current source driven by the op−amp). In case of very high load current, the sense current attains its maximum value defined by the capability of the internal current source. Any further increase in the load current does not increase the sense current and therefore, the sense ratio starts to deviate even if sufficient voltage headroom is available for the operation of internal analog circuit elements. This maximum sense current is typically defined well below the lower limit for the fault state sense current, and is specified in the product datasheets.

The discussion above suggests that the potential at the CS pin may rise all the way up to V_{BATT} in certain situations. This could potentially stress/damage the A/D stage of the microcontroller, especially in cases of high battery voltages. To prevent such a scenario, an external clamp, Z_{CS}, is recommended as shown in Figure 49. The resistor R_{SENSE} limits the current through Z_{CS}. The RC network comprising of $R_{A/D}$ and C_{CS} is the recommended low pass filter for the input A/D. The values for these components are specified in the datasheets, and may also be chosen by the customer to fit the requirements of their respective A/D stage.

CS Enable/Disable Logic

Different logic topologies may be used within **onsemi** High−Side Smart FETs for enabling/disabling the analog current sense output. For instance, NCV84160 employs a Current Sense Disable logic input that disables (turns off) the CS output on receiving a Hi (logic level) command signal. In other words, follows an active low logic for CS operation. Other devices, such as NCV84140 and NCV84012A have an active high Current Sense Enable logic input that turns on the CS output on receiving a Hi (logic level) command signal from the microcontroller. In multi−channel devices where the CS outputs are multiplexed through a select input pin, the Enable/Disable logic is common to all the channels (See Figure 14). For current sense enable/disable philosophy for a specific device, refer to the corresponding product datasheet. The signal conditioning circuitry, logic levels and hysteresis for CS Disable/Enable pin is similar to that for the input pin. Section Input Control and Hysteresis deliberates on the input control logic and signal conditioning. The ESD protection diode, Z_{ESD}, to GND (See Figure 21) limits the potential observed at this pin and also provides protection in case of a reverse battery situation. It is recommended to use a protection resistor while interfacing this node to the microcontroller (See R_{DEN} in Figure 49).

Current Sense Accuracy Improvement at Light Loads

An accurate estimation of load current requires an accurate measurement of sense current and a stable sense ratio over the desirable range of loads. While the former concern is central to the accuracy of the measurement system (the onus of which lies with the application user), the latter is more of a device design challenge. This challenge compounds at small load currents (referred to as light load condition) where the voltages across the FET (Drain−Source and Gate−Source) become comparable to the process offsets and mismatches. Following equation summarizes the two major concerns at low load currents:

$$SR_{Err} = \frac{1}{\left(1 + \frac{V_{OFF}}{V_{DS}}\right)} \cdot \frac{1}{\left(1 + \Delta \frac{V_{th}}{V_{OV}}\right)} \qquad \text{(eq. 11)}$$

Where,

SR_{Err} is the error factor associated with the Sense Ratio, V_{OFF} is the input offset of the op−amp (See Figure 51), and ΔV_{th} is the threshold mismatch between the power and the sense FETs.

As per Eq. 11, the error factor in the sense ratio is dependent on the input offset of the op−amp (that forces the two source nodes together) and on the threshold mismatch in the two FETs.

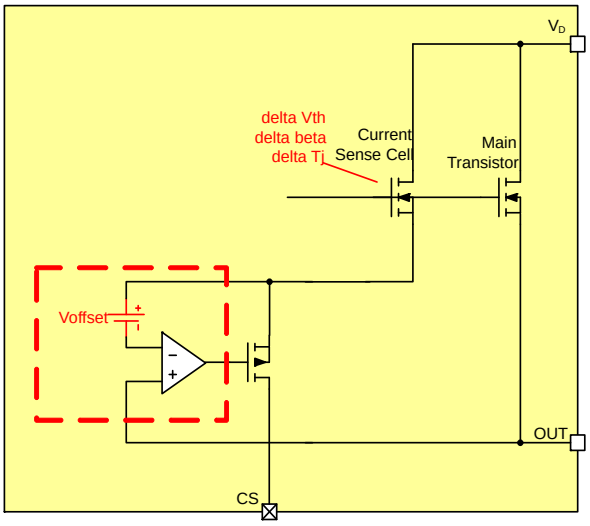

Figure 51. Circuit Schematic Depicting Error in Sense Ratio Due to Op−Amp Offsets and Process Mismatches

At light loads, the drain−to−source voltage of the power FET droops too low and is at par with the op−amp input offset voltage making the first factor in Eq. 11 dominant in the determination of sense ratio. Depending on the polarity of the op−amp offset, the sense ratio may diverge above or below the nominal value.

To alleviate the above issue, a “De−Saturation” circuit is employed that pulls down the charge pump and cuts back the gate voltage, thereby, increasing the $R_{DS\ (ON)}$ (and hence, the V_{DS} drop) of the device. The increased V_{DS} drop mitigates the associated error factor. If the load current is further reduced, the gate voltage is further reduced to get a constant Drain−Source drop below a certain threshold for light loads. The parameter, termed as “Output Voltage Drop Limitation”, and the corresponding light load threshold can be looked up in the specific product datasheet. Since $R_{DS(ON)}$ at such light loads is less of a concern, the on state resistive drops are traded off for improving the current sense accuracy. Figure 52 explains the variation of Drain−Source and Gate−Source voltages in the De−Saturation mode.

At high load currents, the Gate−Source voltage is driven high to the maximum capability of the charge pump, and the Drain−Source voltage scales linearly with the current− In essence, the device behaves like a low ohmic resistor. Below a certain threshold of load current (i.e. the light load condition), the Gate−Source voltage is pulled down and the Drain−Source voltage thereafter is fixed at a level− V_{SAT}. In this region, the device is operating in the linear, or non−$R_{DS(ON)}$ mode and load current bears a square−law relationship to the Gate−Source voltage. The mechanism is therefore called as De−Saturation. The current reduces to zero (in practice there is some minimal subthreshold leakage) once the Gate−Source voltage droops below the threshold voltage, V_{TH}.

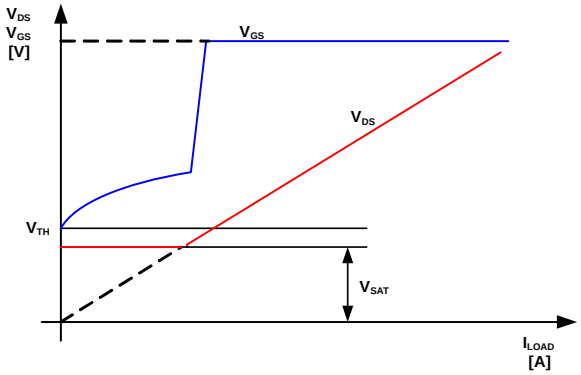

Figure 52. Variation of Drain−Source and Gate−Source Voltages in De−Saturation Mode

Below are the example characterization curves for a High−Side Smart FET in De−Saturation mode depicting the temperature dependence.

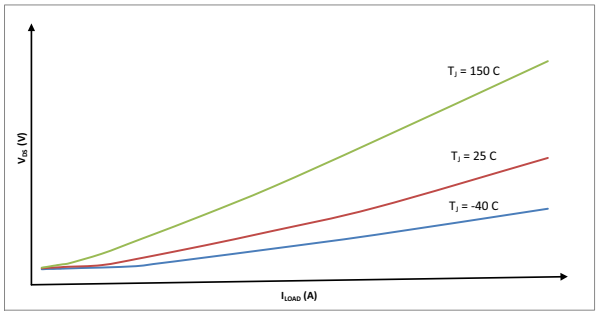

Figure 53. VDS Dependence on Load Current Across Temperature

The Output Voltage Drop Limit is pretty stable across temperature. The threshold current changes because of a change in $R_{DS(ON)}$ with temperature.

The idealized plot below delineates the improvement in sense ratios with the De−Saturation mechanism:

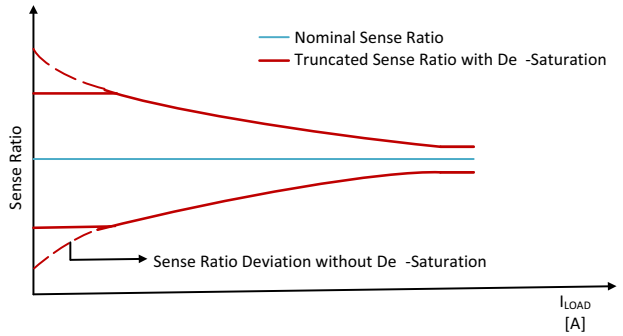

Figure 54. Improvement in Current Sensing Accuracy with De−Saturation

While the approach described above reduces the Sense Ratio error associated with the op−amp offset, a reduction in Gate−Source voltage would make the second factor (Refer to Eq. 11)− threshold mismatch, dominant in determination of the error. As the gate voltage is reduced, the overdrive for the two FETs becomes comparable to the mismatch in the threshold voltages which once again deviates the Sense Ratio from its nominal value. In order to achieve superior current sense accuracies at light loads, the new family of High Side SmartFETs, such as NCV84008A, NCV84012A etc. employ a split FET control current sensing mechanism instead of de−saturation. The principle of operation is depicted in Figure 55. The predicament in the form of a dominant op−amp offset at light loads is addressed by turning off a part of the power FET instead of regulating it at low gate voltages. The required increase in $R_{DS(ON)}$ (which subsequently increases the V_{DS} compared to the offset) at light loads, is therefore, achieved without driving the output stage at low gate overdrive voltages which eliminates the V_{th} mismatch error. The sense output is also scaled at light loads to maintain a constant current sense ratio per the spec. A major challenge with such a mechanism is to define the ratio of the output FET “fingers” to be switched off as well as ensuring synchronization of the split fingers especially under stressful conditions such as current limit. Since the V_{DS} of the power FET scales with the output current at light loads (unlike de−saturation where a constant V_{DS} is attained per Figure 55), the threshold for light load operation is defined in terms of output current instead of the output voltage drop limitation. In case of the conventional de−saturation mechanism, it is desirable to have the two FETs closely matched to reduce any threshold related offsets. The architecture of the fault reporting circuit (Figure 55) is not altered between the two different light load accuracy improvement techniques.

It is to be noted that the sense ratio also drifts with temperature and load currents (especially at lighter load currents). A calibration routine described in section Current Sense Calibration helps in improving the accuracy over the desired load current range.

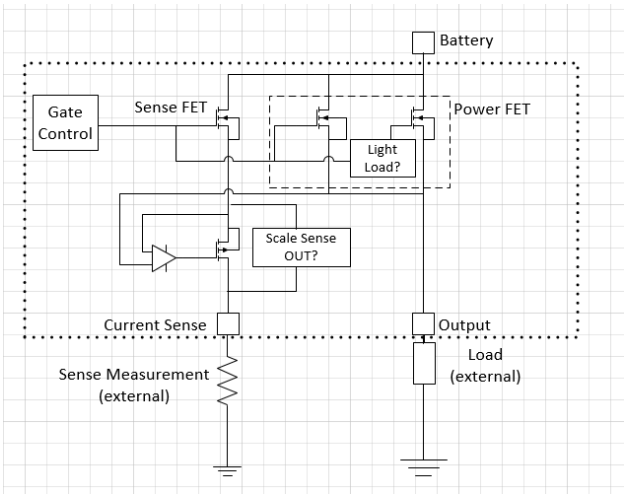

Figure 55. Split FET Current Sensing Mechanism

Current Sense Behavior in Normal and Fault States

Normal State Operation

During normal operation, the sensed current output (or the voltage sensed across the sense resistor) is proportional to the load current. For a reasonably sized sense resistor (See CS Pin Interface and Sensing the Current), the sense voltage at nominal loads is lower than fault state sense voltage to unambiguously detect a fault condition. For devices like NCV84012A, that have the current sense fault level within the range of saturated overload sense current (Refer datasheet), a sense fault level is displayed in the OFF state as well as described in the following sections. Refer to product datasheets for specs on fault and nominal state sense currents and voltages. The timing diagram in Figure 56 mentions the important current sense timing parameters while switching nominal loads.

Unless mentioned otherwise, the CS timing parameters referenced to the Enable/Disable signal are termed as t_{CS_High1}/t_{CS_Low1}; and the parameters referenced with respect to the Input command are termed as t_{CS_High2}/t_{CS_Low2}. The wave−set shown in Figure 56 also depicts the response of current sense signal to changing load currents. The signal DS refers to the Diagnostic Select− this selects the channel to be sensed in case of a multi−channel device. The typical values and range for these timing parameters are mentioned in the respective product datasheets. For any PWM operation, the current sense timings need to be considered in addition to the device turn on and turn off timings. The frequency of the PWM operation must not exceed the CS switching capability to ensure reliable current sensing and diagnostics.

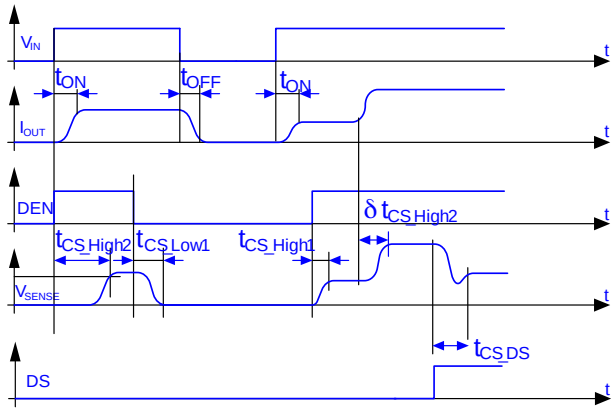

Figure 56. Current Sense Timing With Nominal Load Switching

Open Load Diagnostics

OFF State

Under normal conditions in off state, when the input command is Lo, the output should be pulled down to GND by the load. An open load condition will exist in case the connection to the load is lost, or the load itself wears out into a high impedance stage (for e.g. a broken array of series LED string). Such a condition will be detected and flagged by the device as a fault. The analog current sense pin in such an event will output the fault state current−typically higher than the currents sensed during normal operation and a high fault−state sense voltage will be sensed across the sense resistor. Figure 57 explains the Off State Open Load detection mechanism.

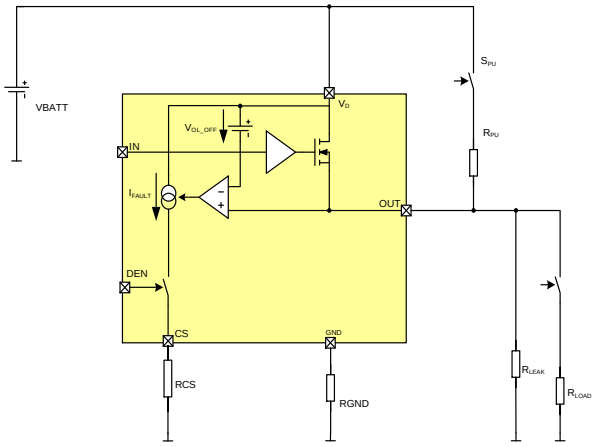

Figure 57. Off State Open Load Diagnosis Principle

In an automotive environment, an “absolute open load” condition would almost never exist, i.e. there will always be some leakage path to GND (attributing to temperature, humidity, system parasitics etc.) even if the load is open. This impedance is represented by R_{LEAK} in the figure above. A potential is thus developed at the output node which is then sensed by a comparator and compared against a threshold voltage. An external pull−up resistor, R_{PU} is recommended to be connected to the output terminal which, in case of an open load, pulls up the output node to battery and ensures the detection of an open load. This resistor is typically complemented by a switch, S_{PU}, to avoid the undesired leakage through R_{PU} when open load detection is not required.

The value of R_{PU} needs to be selected after considering the typical application loads, system parasitics and leakages in off state (R_{LEAK}). It should be sized such that the voltage at the output node (or the potential divider created by R_{LEAK} and R_{PU}) should be sufficient to flag an open load fault. Towards this approach, there will be a max limit to R_{PU}. In addition, the resistor should be able to handle the power dissipation which puts a minimum limit to R_{PU}. For specific R_{PU} recommendations for a device, refer to the product datasheet.

The comparator network mentioned above is designed to have a high input impedance stage interfaced to the output node to reduce the leakages associated with the open load detection circuit. Typical Off State Open Load leakage levels in **onsemi** High Side SmartFETs are < ± 10 μA (Refer to product datasheets for specs). It should also be noted that the output voltage in this circuit is being compared against

a threshold referenced to V_{BATT}. In other words, this threshold will scale with the battery voltage and will always be certain volts lower than the battery voltage. For instance in NCV84012A, the typical output threshold voltage (for open load detection) is 1.3 V to 2.3 V below V_{BATT}. This design topology may not be true for all **onsemi** High Side SmartFETs. In NCV84160, for e.g., the output threshold voltage is referenced to ground and is typically in the range of 2 V ~ 4 V irrespective of the battery voltage (as long as V_{BATT} is within the recommended operating range). For such devices, the voltage at the comparator's negative input in Figure 57 is referenced to GND. The current sense output current in case of open load fault is generally similar to that in case of ON state faults (such as in case of current limit). Some devices, like NCV84012A, offer fault differentiation in the form of different CS output current levels corresponding to different application failure modes. Product datasheets describe the range of CS output current for different faults. Refer to product datasheets for specific information on open load detection.

Once an open load is detected, the fault state current source (Figure 57) will override the CS output. There is always a finite delay time before the current sense output is flagged high as depicted in the idealized wave−set in Figure 58. The off−state open load timing and control logic spec differs across devices. NCV84160, for example has a typical delay timing spec of 350 μs whereas NCV84012A has this parameter specified at a typical of 70 μs. Further, the latter device incorporates a counter based fault differentiation in OFF State. The counter based retry methodology is explained in Section Re−try Strategy**.** If the counter value is non−zero at the time of externally disabling the device (V_{IN} : Hi → Lo), it is implied that a fault in the form of over−load/ over−temperature was present in the preceding switch ON cycle. In such case, the respective ON State fault output takes precedence over the OFF state fault until the counter reset conditions (described in the product datasheets) are satisfied. This is done to provide fault information to the microcontroller in OFF state before it attempts to enable the SmartFET again, for instance in a PWM operation. OFF State faults, while critical to diagnose, are not as detrimental to the device as repetitive overload/over−temp conditions and are therefore given a lower priority than the latter. In case the counter is zero in OFF state, then the CS output is determined solely by OSOL fault being present or not.

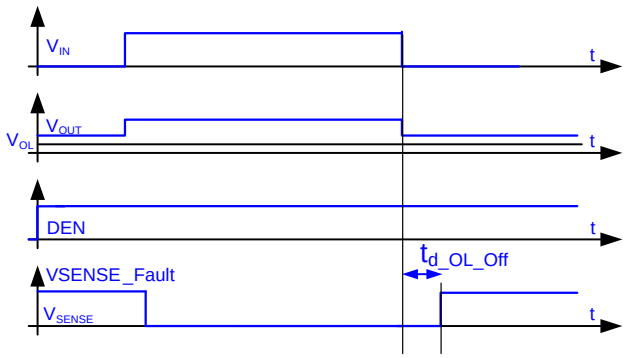

Figure 58. Off State Open Load Delay Timing

ON State

When the input command to the device is Hi, the output is pulled up close to V_{BATT}. If no load is present, minimal leakage current flows (typically < 50 mA) through the device as discussed above. The sense current and therefore, the voltage sensed across R_{CS} are also small, and have been approximated as zero in the idealized wave−set in Figure 58. Such low sense currents make it challenging to distinguish between an underload and open load condition. Further, while driving an LED load, where the drive currents for the LED could be in milli−Amps, it could again be difficult to unambiguously differentiate open load from a nominal LED load. Deviation from nominal sense ratios at these small load currents adds to the difficulty in detection of an open load during on state.

Short Circuit to Battery

A short circuit to V_{BATT} at the output can be detected by the same circuit discussed above for off state open load diagnosis by adding a pull down resistor, R_{PD} externally as shown below in Figure 59.

The pull down resistor differentiates an off state open load (in which case the voltage at the output node is created by the R_{PU}−R_{PD} potential divider) from a short circuit to V_{BATT} (where the voltage at the output node is equal to V_{BATT}, assuming a perfect short). In either case, the comparator will detect a fault and the voltage sensed at the output can be used for discriminating analysis. In addition, this resistor also provides a path to GND in case of a floating output node. In on state, the load current will be zero (in case of an ideal short), or extremely small (in case of a resistive short to V_{BATT}). The sense currents would consequently be small as

well posing a similar challenge as discussed in open load during on state.

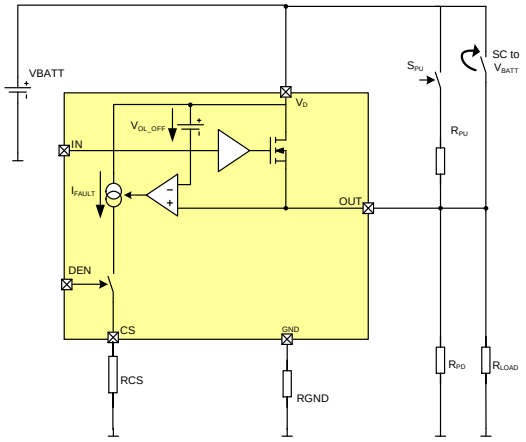

Figure 59. Short Circuit to V_{BATT} Detection

Current Limitation

As discussed in section Short Circuit OUT to GND−Current Limitation, all **onsemi** High Side SmartFETs are equipped with a current limiter circuit that protects the device in case of overload situations by limiting the maximum current through the device. An overload situation is detected by the device as a fault condition, and the sense voltage is correspondingly flagged high. The circuit schematic in Figure 60 describes the principle of operation.

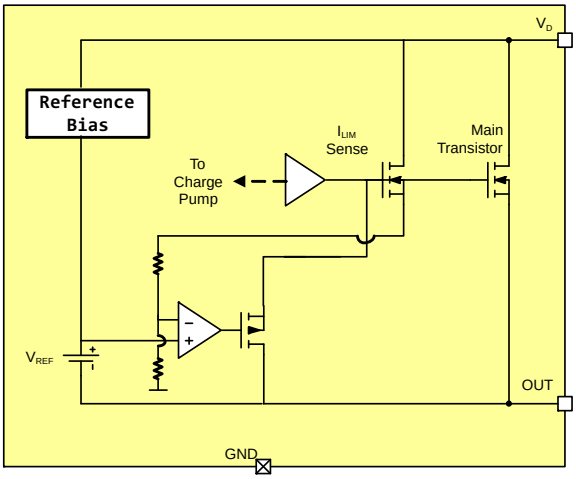

Figure 60. Current Limitation−Operating Principle

The ILIM circuit block includes a sense FET (different from the regular current sense FET) feeding a comparator. When the load current reaches a certain threshold known as I_{LIM} (characterized as a voltage V_{REF} here), the gate voltage is pulled down as shown above. The I_{LIM} circuit block will override the charge pump. The device will no longer be operating in the $R_{DS(ON)}$ mode and will output a maximum saturated current. A separate sense device for current limitation isolates the CS output from this block, thus providing a stable current sense output. The I_{LIM} operation is very similar in principle as the De−saturation mechanism. The former becomes active in case of an overload, and the latter comes into operation at light loads. Some devices, as discussed in section Short Circuit OUT to GND−Current Limitation, may have a peak detect based current limit protection with a timer/counter−based retry strategy. The fault diagnosis in these devices is not different from the ones that employ linear current limit regulation. There are however some subtle differences as highlighted in the next section. The current sense response in case of an overload situation is depicted in the idealized wave−set in the next section in a short circuit to GND event.

Short Circuit to GND

In a short circuit to ground event, the output current gets limited by the current limiter mechanism explained above. When the differential temperature of the die exceeds the set threshold, the device turns off and then toggles until the short circuit condition persists and/or the input command is Hi. The current sense output is as below:

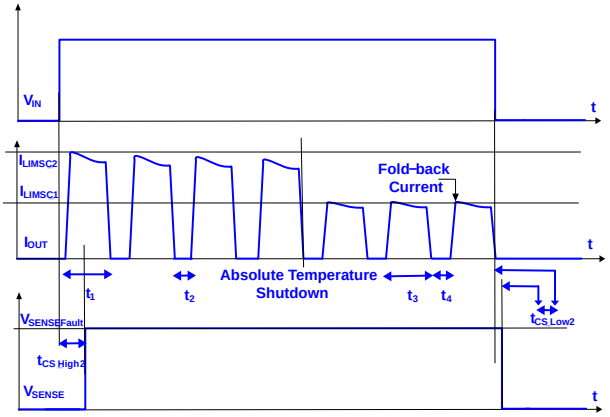

Figure 61. CS Behavior in a Short Circuit to GND Event

The CS timing parameters are similar to the ones discussed in section Normal State Operation. The example here considers a device with fold−back current post absolute thermal shutdown. The current sense response would, however, be similar for a device with no fold−back. As the device successively goes into thermal shutdown followed by another I_{LIM} pulse, the current sense should not toggle and the CS pin should output a stable fault−state current/voltage. For this purpose, the hysteresis of the current sense output is designed to be greater than that for the output current. This characteristic will be discussed using the waveforms in the next section. In practice, as the device heats up during a short circuit event, the current sense output may reduce slightly in amplitude (because of a slightly negative temperature coefficient). Also, with the high current pulses, the battery voltage may droop transiently (depending on supply's series impedance). In such case, the current sense output will follow the battery and may droop transiently. In both the

scenarios, the CS droop is minimal and will not affect the digitized current sense readout (for fault indication) at the microcontroller.

In devices with a counter based retry strategy, such as NCV84012A, the current sense transitions in case of a transient short circuit to GND are depicted in Figure 62. As a current limit peak is detected in short circuit, the internal counter is incremented and the sense output flags a fault. For more information on timing parameters, refer to section Re−try Strategy. As the short circuit is removed and a nominal load is connected, the output transitions into I_{NOM}. The current sense, however, stays at the fault level for a time defined as the blanking period. This feature is also present in devices with linear current limit and is employed to prevent successive fault to nominal transitions in current sense in case of intermittent short circuit to GND such as physical wire de−bouncing. It should be noted that the current sense fault level in SmartFETs like NCV84012A may be lower than that in case of overload conditions (Refer to product datasheet for sense fault current range). Once the input command is disabled, the current sense once again displays the current limit fault encountered in the preceding ON cycle. The fault is displayed until the reset condition in the form of a diagnostic enable pulse is forced. The other reset condition forced by input enable is presented in Section Re−try Strategy. If an open load fault is present, the corresponding fault level at sense output will be present after the counter is reset. Refer section Open Load Diagnostics for details.

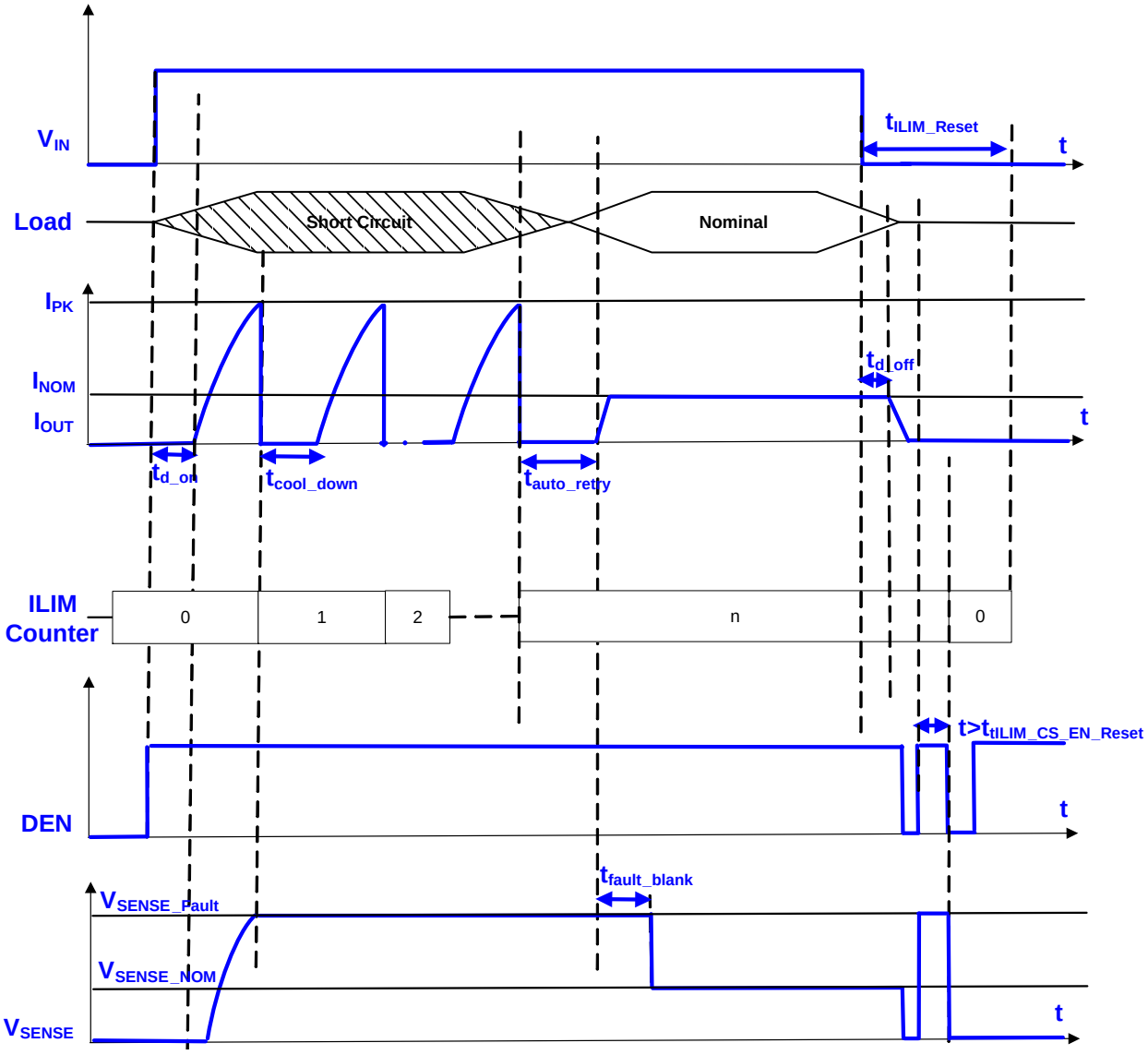

Figure 62. CS Behavior in Counter Based Retry Strategy

Over−temperature Operation

If the differential temperature, or the absolute temperature of the die exceeds the set threshold (Refer section Temperature/Power Limitation), the device protects itself and goes into thermal shutdown. The current sense outputs a fault state current in case of a thermal shutdown event. The operation in this regime is depicted using an exemplary bulb turn−on scenario.

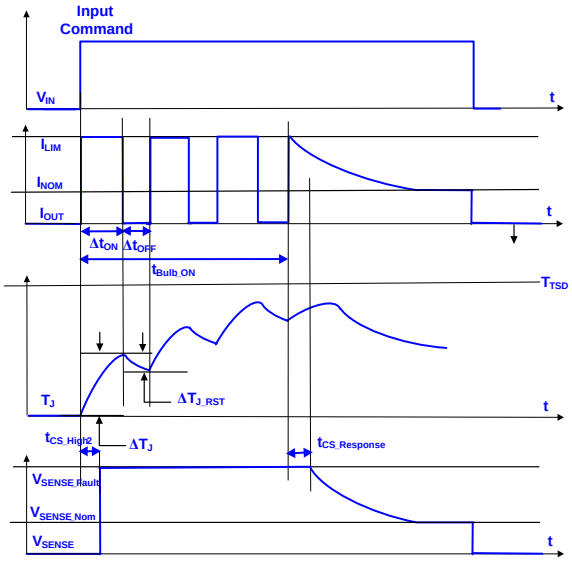

Figure 63. Thermal Toggling During Bulb Turn−On

Assuming that the ambient temperature (at t = 0) was not high enough to trigger absolute thermal shutdown, the device goes into a current limitation operation mode as it tries to turn the bulb on. The current sense flags a fault for overload and the device subsequently undergoes thermal shutdown followed by another I_{LIM} pulse, and so on. The current sense output stays Hi indicating the fault state. As the bulb turns on and the device transitions into normal operation, (for details on bulb turn on, refer to section Bulb Loads) the temperature of the die reduces and current sense output follows the load current trajectory. The time $t_{cs\_Response}$ can be considered as the “thermal hysteresis” of the CS output. In other words, the current sense output stays Hi for some time after the device moves out of a fault condition. This eliminates the unnecessary toggling of the current sense output in case of I_{LIM} and thermal shutdown events. This response time is only for diagnostic purposes and bears no correlation to the ability of the device in turning on a bulb. For specs on typical $t_{cs\_Response}$ times, refer to the specific product datasheet. It should be noted that the CS output transition from nominal to fault state may not be as “smooth” as depicted in the idealized wave−set above. This transition involves turning off of the fault state current source and turning on the nominal state CS circuit (Refer Figure 46), and may exhibit sporadic noise spikes during this switching. Nonetheless, these high frequency spikes will be easily filtered by the RC network (Figure 49) preceding the microcontroller’s A/D stage, and thus will not affect the digitized current sense output.

Underload

Sections Short Circuit to Battery and Current Limitation discuss the challenge while discerning an underload condition from an open load and/or SC to V_{BATT} during on state. Some devices, NCV84012A for instance, distinguish the underload condition by forcing a sense current < I_{Load}/K_{Nom} (the nominal sense current at that load) below the output current threshold defined for the underload. For small load currents, the sense ratio accuracy deteriorates and makes it difficult to recognize if the low level of sensed current indicates an underload condition, or is it the deviation in the sense ratio that is misleading in the estimation of load current when the true load current is above the underload threshold. The threshold for underload should be carefully set considering the open load impedance, intended application nominal loads and the device leakage. On one hand, there should be sufficient margin between the underload and open load thresholds so that the sensed current can distinguish between the two (with reasonable CS accuracy); and on the other hand the underload threshold cannot be set too high considering the loads such as LEDs require low nominal drive currents. For typical thresholds, refer to the specific product datasheets.

Current Sense Calibration

While **onsemi** High Side SmartFETs are designed to offer stable sense ratios, some inaccuracy is bound to be present because of the offsets in the analog circuitry (refer section Current Sense Accuracy Improvement at Light Loads) and drifts with temperature, stress and load current. The tolerances and drifts are mentioned in the respective product datasheets. To further reduce these tolerances, a convenient calibration scheme can be performed at the EOL (End of Line) testing by the ECU (microcontroller) manufacturer. Before discussing the calibration procedure, the “problem statement” and the associated challenge is presented below.

With an ideal sense ratio, the relationship between the sense and output currents is described as:

$$I_{SENSE} = \frac{1}{SR} \cdot I_{OUT} \qquad \text{(eq. 12)}$$

Representing this graphically,

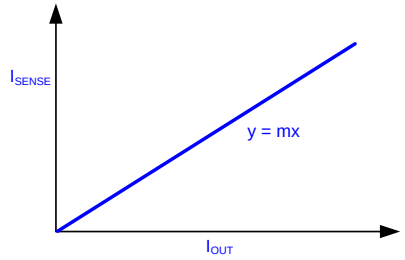

Figure 64. Sense Current vs Output Current With An Ideal Sense Ratio

The slope of the line is given by the sense ratio. The offsets of the analog circuitry (Refer Eq. 11 From sections Current Sense Accuracy Improvement at Light Loads) manifest themselves as a sense offset current. In other words, there would be a finite sense current flowing out of the CS pin when the load/output current is essentially zero. This can be modelled as:

$$I_{SENSE} = \frac{1}{SR} \cdot I_{OUT} + I_{OFF} \quad \text{(eq. 13)}$$

where I_{OFF} is the offset current. This offset varies from one device to another and also has a temperature dependency. The graphical representation is depicted in Figure 65. The curves in red have the offset errors included. The curvatures at small load currents (where the curve deviates from a straight line equation) are the improvements rendered by the De−saturation or Split−FET control circuit. With no accuracy improvement technique, the sense current would exhibit a higher deviation at low load currents.

The divergence at further reduced load currents arises (primarily) because of the threshold variation between the power and sense FETs.

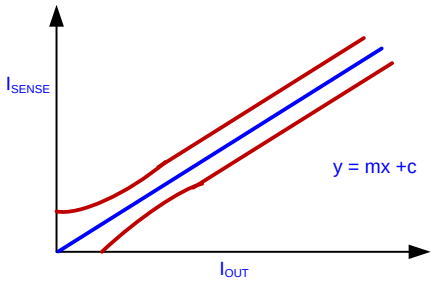

Figure 65. Sense Current vs Output Current With Offset Error and De−Saturation Mechanism

It should be noted that the current coming out of the CS pin is always positive. Therefore the bottom curve does not indicate a negative sense offset; rather it just signifies that in case of negative op−amp offset, a certain load current level needs to be achieved before getting a finite sense current out of the CS pin.

In addition to the offset error, the sense ratio may digress from its nominal value across supply and load current range, and device−to−device variability. Graphically, this can be modelled as a slope error associated with the curves above, and is more pronounced at high load currents. Figure 66 shows the boundary condition curves with the maximum and minimum slope errors.

$$I_{SENSE} = \frac{1}{SR'} \cdot I_{OUT} + I_{OFF} \quad \text{(eq. 14)}$$

is the sense ratio inclusive of the slope error.

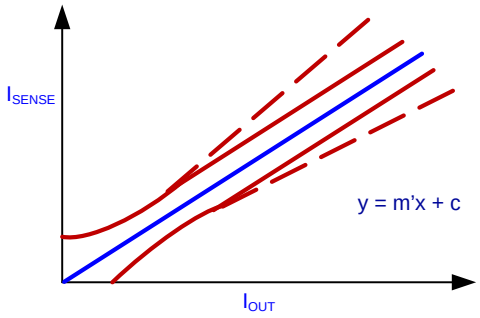

Figure 66. Sense Current vs Output Current With Offset And Slope Error Boundary Curves (see dashed plots)

Both these errors are temperature, load current dependent and device dependent. Further, due to continuous temperature cycling, power cycling and stressing the device, the CS Ratio “drifts” over temp and lifetime. This drift is also load current dependent, and is usually guaranteed by design. Product datasheets typically define and tabulate default maximum and minimum sense ratio and/or sense current at a given load current. This window includes contribution from both the offset as well as slope errors, and essentially represents an I_{SENSE}− I_{OUT} curve similar to Fig 6.19. Any part shipped out of the factory will have an overall accuracy within the bounds of the tolerances specified at different load currents.

In order to understand the implications of these errors, an output current level− I_{OUT1} is chosen.

Ideally, the sense current at this load, is given by I_{SENSE1} (See Figure 67). However, due to inaccuracies in the sense ratio, as discussed above, the sensed current could be anywhere between the boundary curves which leads to an error in the estimated load current between $I_{OUT1'}$ and $I_{OUT1''}$.

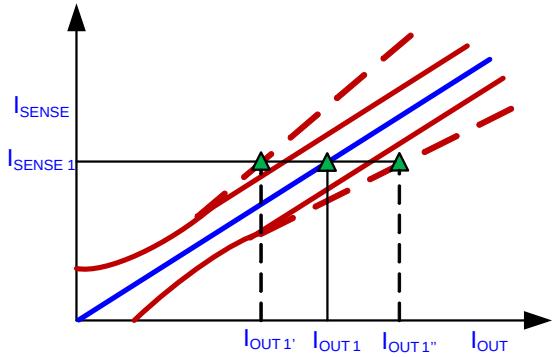

Figure 67. Error In The Estimated Load Current With Inaccuracies In Sense Ratio

At low load currents, the boundary conditions will change with the flipped polarity of the slope error (Figure 68). Nonetheless, the challenge (in accurate estimation of load current) would be similar as discussed above.

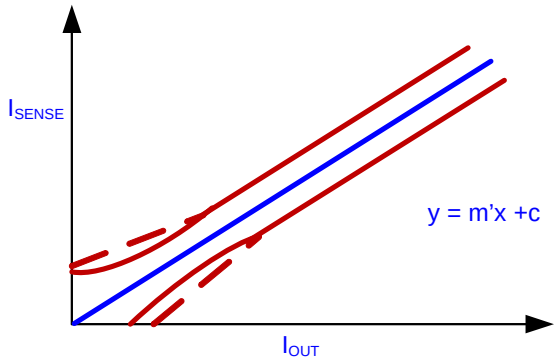

Figure 68. Sense Current vs Output Current With Offset And Slope Error Boundary Curves For Light Loads

With the default current sense accuracy (as published in the product datasheet), there could be a significant error factor in the estimation of load current. The calibration routine at EOL helps improving current sense accuracy over the desired load range. This procedure involves measuring the sense voltages at two known output currents and then recording this data in the non−volatile memory of the microcontroller. Since, in the final applications, a sense voltage would be “measured” and a load current would be “estimated” thereafter, the Eq. 14 above need to be re−arranged as follows:

$$I_{OUT} = \frac{SR'}{R_{SENSE}} \cdot - I_{OFF} \cdot SR' \qquad \text{(eq. 15)}$$

This can be represented by the straight line equation below.

$$I_{OUT} = m_1 \cdot V_{SENSE} + c_1 \qquad \text{(eq. 16)}$$

Where $m_1 = \frac{SR'}{R_{CS}}$ and $c_1 = - I_{OFF} \cdot SR'$

Measuring two points on this line would render the values of slope and intercept for a particular device. Once these values are known for a device, the output current can be estimated, with reasonable accuracy, for any other load by measuring the sense voltage and substituting the calibrated slope and intercept. Since the calibration routine is generally not performed across a temperature range (to save test time, resources and microcontroller memory overheads), the drift error associated with the sense ratios would still be present. Considering the current sense measurements in NCV84045 as an example, the current sense ratios are specified as follows:

Table 2. Current Sense Ratio Spec− NCV84045

Load Current (Amp)	Sense Ratio		
	Min	Typ	Max
0.05	350	1455	1800
0.5	500	1330	1740
0.7	760	1290	1630
1.5	970	1200	1420
4.5	1090	1190	1340

Now, measuring the current sense voltage at two load currents, for instance, at 0.5 Amp and at 4.5 Amp and subsequently putting in those values in the equations below, slope and intercept can be calculated.

$$\left.\begin{aligned} m_1 &= \frac{4.5 - 0.5}{V_{SENSE2} - V_{SENSE1}} \\ \text{and } c_1 &= 0.5 - m_1 \cdot V_{SENSE} \end{aligned}\right\} \qquad \text{(eq. 17)}$$

The calibration routine requires these slopes and intercepts to be stored in microcontroller’s memory. This equation is then used to estimate load currents by measuring sense voltages at those loads, thereby eliminating the slope error and intercept error. The current sense drift across temperature cycles and stress over lifetime still persists. The table below summarizes the current sense drift spec in NCV84045. This table implies that, once calibrated, the allowed drift over power and temperature cycling across lifetime is within the specified tolerances that are equivalent to the relative errors in the estimation of load current from the measured sense voltage.

Table 3. Current Sense Drift Spec in NCV84045

Load (Amp)	Current Sense Drift	
	Min	Max
0.05	−25	25
0.5	−20	20
0.7	−15	15
1.5	−10	10
4.5	−5	5

It should be considered that the temperature variability and tolerance of sense resistor has not been accounted here which will add to the error factor associated with estimated load current. Further, the temperature drift of offset error, though minimal, has also been ignored. The calibration routine, thus, offers a significant improvement in load current estimation. In some cases (where the overall test time at EOL needs to be reduced), a one point calibration could also be performed. In this technique, the slope in

Eq.14 (which is inversely proportional to the differential sense ratio estimated from the I_{SENSE} − I_{LOAD} curve) is “assumed” as typical (defined by the centered CS ratio per the spec), and the intercept is calculated by a single measurement point assuming typical slope. The current sense improvement rendered by this technique, however, is not as good as the two point calibration method discussed above.

UNDERSTANDING THE THERMAL NETWORK

Understanding and accurate estimation of a device’s thermal response has been a long standing challenge with regards to the automotive applications where external conditions can vary in extremes. Thermal overstress, in the form of transient or continual temperature swings, exceeding device’s thermal capacity is one of the most encountered failure modes in the field, especially for power devices that frequently observe these transients through their lifetime. Further, with the continuous miniaturization of silicon feature geometries, die and packages sizes, the likelihood of generating “thermal fractures” increases. This necessitates a comprehensive understanding of the thermal response of the device and the influences of the external factors such as the device mounting conditions, application boards, peripheral heat sources/sinks etc. From a design’s point of view, the layout, structure and the protection features (incorporated in the device) should be designed considering the implications on the thermal performance in the target application. This section describes the contribution of the above mentioned internal and external factors in determining and/or achieving the desired thermal behavior in the system. In addition, the associated metrics that quantify the thermal performance and the corresponding exemplary datasheet specifications will also be explained in this section. Lastly, the design philosophy of protection features, such as current limitation and thermal shutdown (both absolute and differential), vis−a−vis the thermal ameliorations rendered will be discussed.

Thermal Resistance− Physical Interpretation

Transient as well as steady state thermal resistance is the parameter readily used in the semiconductor industry to quantify the thermal performance of a device. This parameter is usually specified in the product datasheet under a certain set of conditions (refer section Datasheet Parameters and Specifications). While mathematically, the parameter is described as °C/Watt, i.e. the temperature change consequential to the power applied to the device; the physical representation is analogous to its electrical counterpart− a quantity obstructing/resisting the heat flow (analogous to electrical current) by developing a thermal potential (analogous to electrical voltage) across it. Figure 69 depicts the layer by layer structure, or the thermal potential divider ladder in an application.

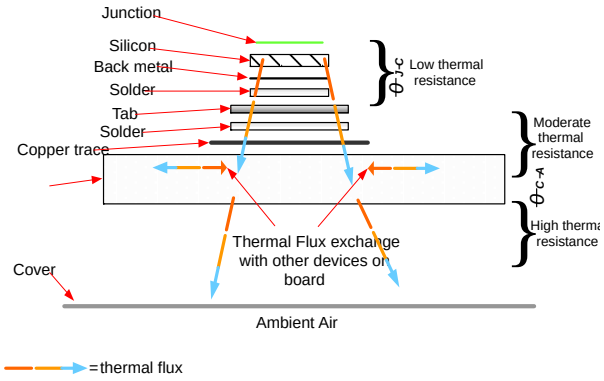

Figure 69. Thermal Resistance Physical Ladder in Application

Before explaining the layer structure above, it is assumed that a power pulse is applied to the device. In such case, the temperature of the device and the “surrounding environment” will increase, and heat will start to flow in the form of thermal flux. Once the power is turned off, the temperature will start to decay and will eventually attain steady state, or equilibrium.

Now, the junction of the device observes maximum temperature swings assuming a uniform current density through the device with no surface defects. Since the junction is confined to rather shallow depths, maximum temperature is observed in the near−surface region. In case of non−uniform current densities, one section of the near−surface region conducts more current thereby creating thermal hot−spots (which may irreversibly damage the die) that make it difficult to model the average junction temperature. The next layer in the path of thermal flux is collectively called as “silicon” which includes the substrate, epitaxial layers and any implants (not in the vicinity of the junction). The thickness of the die plays a critical role in achieving the required thermal performance, especially over short duration power events (as will be discussed later). The thicker the die, the more is the time required for the heat to flow out of the device, and the more is the thermal resistance presented to the thermal flux. This entails a parametric trade−off as a higher epitaxial thickness is required for supporting the required breakdown voltage and ensuring the mechanical stability of the wafer (especially for large wafer diameters). Further, the material of the substrate, presence of any volumetric defects also affects the flow of heat out of the device. For instance, devices realized on silicon−on−insulator substrates may be better in terms of reduced leakages and a lesser likelihood of latch−up, but exhibit a higher thermal resistance than Si substrates. On the other hand, materials like SiC (silicon carbide) exhibit a higher thermal conductivity than Si. Therefore, the material and physical properties of the substrate should be decided considering the desired thermal performance from the final device.

After the substrate, the next layer in the ladder is the back side metal followed by the solder. All products in the **onsemi** high−side SmartFET family have a back side drain contact to manage the high power requirements by distributing the current density over the entire substrate contact area. Choice of metal also determines the thermal resistance. The structure depicted in Figure 69 assumes a back side tab, or an “exposed pad” connection for the drain terminal (which may or may not be present depending on the device and technology). This is usually realized using solder as the conductive die−attach to the tab. The solder layer should be uniform in thickness and conformal to the drain contact. Voids in solder have been a known failure mode leading to high transient thermal resistance. On the source side, power metallization for the source contact and the set of bond wires determine and limit the thermal performance of the device (refer section Improving the transient thermal performance for impact of bond wires). Until the tab layer (inclusive of the lead frame, mold compound and the package), a one dimensional heat flow model is (reasonably) assumed with thermal flux flowing vertically. The thermal resistance until this point is collectively termed as $\theta_{Junction-Case}$, or $\theta_{Junction-Pin}$ (in case there is no back side exposed pad), or $\theta_{Junction-Soldering\ Point}$. Once, the heat starts to flow out of the package, the lateral flux sourced in by any other heat sources in the vicinity of the concerned device need to be taken into account as well, and the model may transpire into a dimensional heat flow network, which is typically more challenging to analyze and estimate. This assumption, however, does not always hold true for multi−channel devices where the adjacent channels could be conducting power and dissipating heat laterally into the die, thus complicating the analysis. After the package layer, the mounting and application conditions determine the thermal resistance. These include the amount of solder, the Cu heat spreader area on the application PCB, the length and width of traces, number of layers in the PCB, any internal planes for heat conduction, characteristics of the epoxy used, if any, between the application PCB and the ECU casing etc. Section Understanding the Datasheet Curves discusses the impact of some of these factors on the thermal resistance of the system. Adding the resistance contribution of all these ladders yields the overall Junction−to−ambient thermal resistance in the application.

The extent of heat flow within the ladder structure discussed above depends on the pulse timings and duty cycle. From empirical as well as simulation results, it is estimated that up to a few 100 μs in a single pulse power event, the die active area, technology and physical attributes determine the thermal resistance and the outside application environment has minimum contribution towards the thermal response over short pulse durations. As the (single) pulse period is increased, the lead frame, package, mold compound etc. begin to have an impact on the thermal performance. This impact is usually pronounced for the pulse periods of a few milliseconds. For longer pulse periods, going up to a few seconds, the application conditions (as described in the above paragraph) have a greater influence on the thermal resistance. As the system reaches equilibrium over long pulse periods (typically more than 100s of seconds), the device itself has minimal contribution in the steady state thermal resistance, and the thermal performance only depends on the test conditions. It should be noted that these time periods are only estimates and assume that the pulse period and the power levels applied are well within the boundary conditions defined for the device and do not interfere with the thresholds defined for the protection circuitry− for instance, thermal shutdown.

Thermal resistance in case of repetitive power pulse events depend on the duty cycle. Depending on the duty cycle, the heat accumulated in a power pulse may, or may not be “carried over” to the subsequent pulse, thereby confounding the analysis. Further, there is a time lag between the electrical power wave and the consequent thermal wave which must be taken into account during the thermal analysis over a repetitive pulse event. See below for the simulated thermal wave for a hypothetical power profile on an exemplary device.

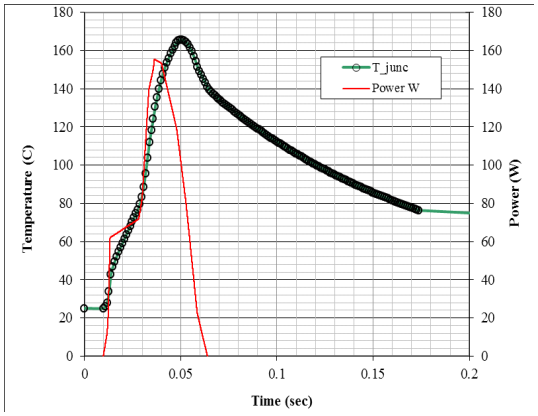

Figure 70. Simulation Depicting The Lag in The Thermal Wave For An Arbitrary Power Profile

Improving the transient thermal performance

As discussed in the previous section, transient thermal resistance over relatively short periods of time (typically limited to a few milliseconds) depends more on the device than on the application conditions. The “device” here includes contribution from both the die and the package. Since the geometrical and physical attributes of the die are primarily driven to optimize performance parameters like conduction losses and breakdowns, there is little scope of any enhancements in the die itself to improve the thermal capability. Package enhancements, on the other hand, are relatively more tenable and can significantly improve the transient thermal performance over single pulse as well as repetitive pulse enhancements.

Certain **onsemi** High−Side SmartFETs (depending on technology and application requirements) incorporate an exposed pad, or tab connection for the drain terminal to

improve the heat dissipation. Figure 71 shows the thermal flux flow through an exposed pad. An E−pad connection offers a superior transient thermal performance over similar sized devices with a pin−out, or a combination of pins for the drain connection (bonded to the back side drain with bond wires).

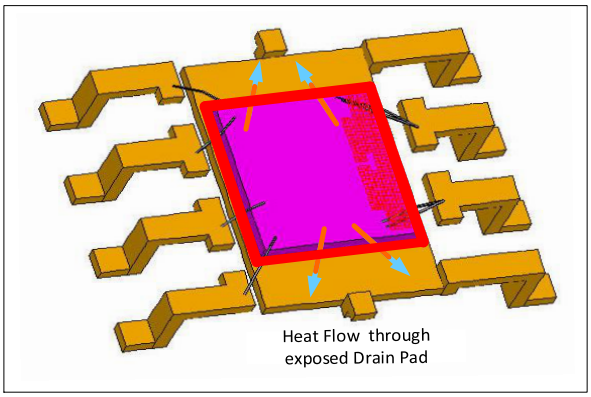

Figure 71. Thermal Flux Flow With The E−Pad For Drain Terminal

With the E−pad, the solder and spreader area on the application PCB is also increased which provides additional heat sinking and helps improve heat dissipation over longer pulse durations (> 1 sec).

In addition to the drain terminal, the other node in the path of the power flow is the source terminal. Source contact, top power metal and bond−out to the lead frame, all have an impact on the transient thermal performance and consequently in determining the maximum power handling capability of the device. Since most of the power dissipation happens over shallow junction depths, it is imperative to consider the thermal conductivity and thickness of the source top metal especially while designing high power density devices. Some of the high power **onsemi** SmartFETs have copper top metal instead of the conventional Al alloy to offer improved thermal resistance. In case of extremely low $R_{DS(ON)}$ devices (such as NCV84004A, NCV84006A etc.), the overhead electrical losses associated with the "back−end technology" including bond wires tend to limit the parametric performance of the device. For such devices, an alternative bonding in the form of "copper clip" provides superior electrical and thermal performance. The clip covers the entire active area of the power FET and instantaneously transfers heat from silicon to the lead frame, thus acting as a top side heat sink.

While beneficial in case of low $R_{DS(ON)}$ high power devices, clip layout and placement is an important concern for the stability of the die in case of high power dissipation. Any unexposed area around the edges of the clips can create a localized hotspot and serve as the site for thermal runaway. Addressing this concern is particularly important in case of monolithic devices that have the control circuit placed next to the control logic with narrow spaces for routing feed−through signals. Laying out a clip and maintaining its conformity over the entire FET area is often challenging. In such cases, other avenues for improving thermal performance are explored− including, but not limited to, changing the top metal stack composition and thickness, increasing the number and/or thickness of bond wires.

Further, for devices with lower power requirements, clip placement faces economic and technological constraints with a small silicon area available for bonding. These devices employ bond wires for drain and source connections to the lead frame. Thermal performance is enhanced by employing multiple bond wires as well as (in some cases) multiple stitches for each such bond wire. Other package enhancements, like improving the mold compound chemistry and optimizing bond parameters to avoid generation of "thermal ruptures", are also applied.

Overall, the bond type and top metal stack are governed by the ease of manufacturability and the required electro−thermal performance from the specific device.

Datasheet Parameters and Specifications

Thermal Resistance−Physical Interpretation describes the physical interpretation of thermal resistance. This interpretation, though imperative for understanding the thermal network, may not be plausible to model, simulate and specify mathematically in the product datasheets to quantify and compare the thermal performance of a device.

Foster and Cauer Networks

For datasheet purposes, for a given die and package, transient as well as steady state thermal measurements are performed in a controlled environment under laboratory setup conditions and thermal resistance is measured by recording the temperature change consequential to a known power pulse. This temperature change is typically measured by analyzing the parametric changes in a pre−calibrated on−chip thermometer, such as the forward drop of a body diode in case of a power FET. This thermometer should be spatially close to the junction and in certain cases is specially fabricated to model thermal profiles. The thermal ground, which is ambient in case of Junction−to−Ambient measurements and case/pin in case of Junction−to−Case/Junction−to−Pin measurements, is kept stable at a fixed temperature through forced convection and heat sinking (to quickly dissipate heat from the system ground). In addition, thermal simulations are performed on the device with available modelling tools such as SPICE, ANSYS etc. Once the measurements are done and plotted, a mathematical R−C model is simulated to fit this measured curve. Figure 72 shows the simulated Foster R−C network.

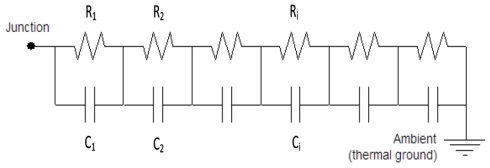

Figure 72. Foster R−C Network Model

The R's and C's are connected such that they yield a time constant unique to each "rung" in the ladder, where:

$$\tau_i = R_i * C_i \quad \text{(eq. 18)}$$

The contribution of each rung is inversely proportional to its time constant, and the rungs with longer time constants have a more pronounced contribution as the system progresses towards steady state. Having stated this, the resistances and corresponding time constants in a foster network, however, have no physical significance, i.e., they are uncorrelated to the physical ladder structure described in section Thermal Resistance−Physical Interpretation. Further, the order and number of rungs in the ladder is also arbitrary and can be changed. In other words, a Foster ladder is a purely mathematical model to fit the measured thermal resistance curve. The more the number of rungs, the better is the precision and the lower is the error factor relative to the actual curve. The advantage of using a foster model is its ease of simulation. Once an R−C network is available for one device, it is relatively easy to create R−C models (and consequently generate transient thermal resistance curves) for other devices in the family by changing inputs to the simulated model− such as device active area for the power FET, total silicon area etc. The sum of the R's in the ladder gives the overall Junction−to−Ambient thermal resistance of the system.

Another type of R−C ladder is the Cauer Network, shown below in Figure 73. In this network, the capacitors are all connected to the system's thermal ground, and the R's and C's in each ladder bear a direct correlation to the physical ladder structure. Intuitively, it can be observed from the ladder that rungs closer to the junction will be charged (thermally) first and the rungs towards the ground will only be charged once the rungs above are saturated with heat. The rungs closer to the junction, therefore, can be related with the device and package, and the rungs closer to the ambient ground can be related to external application conditions (such as PCB), however, with no clear demarcation between the device and its periphery.

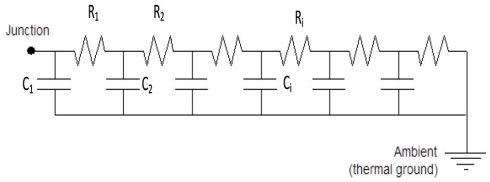

Figure 73. Cauer R−C Network Model

Although the sum of resistances in the Cauer network ladder also yields the overall thermal resistance, the individual rungs are not same as the Foster network. The variations in the system conditions can be better conceptualized by observing corresponding variations in the Cauer R−C network (The relationship between several physical contributors, with similar time constants, and their mathematical equivalents is rather complex). A Cauer network is generally difficult to model and transpose from one device to another, and is generally computed from their Foster counterparts using known algorithms.

The datasheets for **onsemi** High−Side SmartFET family may or may not include these R−C models depending on the specific product. These models, can however, be provided on specific requests from the customer.

Understanding the Datasheet Curves

The datasheets tabulate the steady state junction−to−ambient and junction−to−case/pin/soldering point thermal resistances, unless otherwise specified. Transient thermal resistances are also plotted along with. It should be noted that these resistances are specified against a set of application and mounting conditions such as PCB Cu spreader area and thickness, FR4 area, number of board layers etc. The published curves are valid only under these conditions and should not be used to make junction temperature estimates in case the conditions in application differ from that mentioned in the datasheet. Along the same line of thought, any comparative analysis (within the **onsemi** product portfolio or comparison to competitor devices) will render reliable results only if the test conditions are uniform. Towards this end, certain standards defining the board geometries and properties are followed− for instance JEDEC JESD 51−3, 51−7 etc. Refer to respective product datasheet for the set of conditions followed while describing the thermal resistance. Consider, Figure 74 for example, the Junction−to−ambient transient thermal resistance curve for NCV84160:

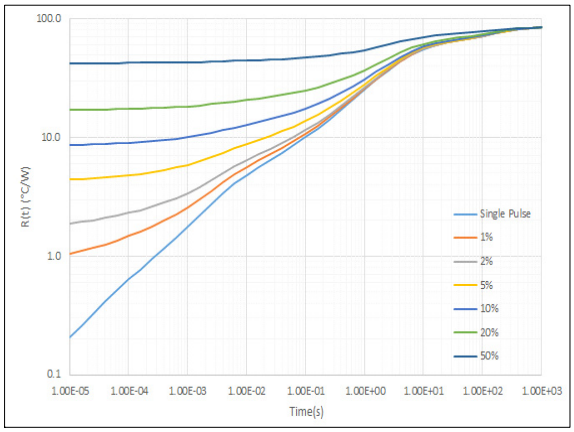

Figure 74. Transient Thermal Resistance Exemplary Curve NCV84160

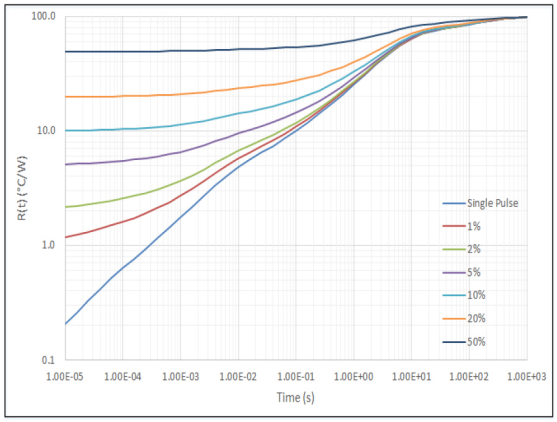

Figure 75. Transient Thermal Resistance Exemplary Curve−NCV84160 For Min Pad Front Cu Area

It should be noted that terms θ and R(t) are interchangeably used to describe the thermal resistance of a device. The curve above plots the thermal resistance over a single pulse as well as a PWM power pulse train (defined by a duty cycle). The measurement conditions specify a single layer PCB with an FR4 area of 4.8 cm *4.8 cm, a front 1 ounce Cu spreader area of ~ 200 mm^2 (generally accounted only for drain and source terminals), back side plane covered with 1 ounce Cu spreader with no internal planes. In addition, it is assumed that no other heat source is operating in the vicinity of the device under test that could potentially influence the thermal profile of the system. The length of traces/test wires, placement of vias (if any), and orientation of the test board and stability of ambient temperature (usually achieved through forced convection) are also known to impact the thermal response, amongst many other factors. The thermal resistance spec is, therefore, valid only under the above mentioned conditions, and cannot be applied universally to any other application condition. To quantify the effect of change in application conditions, the curve in Figure 75 depicts the thermal resistance for the same device (NCV84160) under same conditions as above except that the front Cu spreader area is changed from 200 mm^2 to min pad (with Cu area present only at the soldering points for the package pins).

The steady state thermal resistance increases by ~16%, in this case, for a 200 mm^2 reduction in front Cu spreader area. As another example, a ~75% increase in the FR4 area is expected to yield a ~7% reduction in the steady state resistance (FR4 properties are generally associated with really long time constants per Figure 73, and a perceived impact is evident only for longer pulse durations). The data presented here is valid only for this particular scenario and should not be extended to other devices for which the test conditions and the corresponding impact on thermal resistance may vary.

Assuming that in a particular application, the test conditions are identical to those specified against the published curved in Figure 74, an approximated calculation is described below to estimate the average junction temperature in a hypothetical inductive switching environment.

Consider that a 1 mH inductor is switched with a peak current of 5 Amp at an ambient temperature of 25 °C and a battery voltage of 14 V. The series resistance in the output conduction path has been ignored (may not necessarily be true in the real application). The scenario is depicted in the idealized wave−set below:

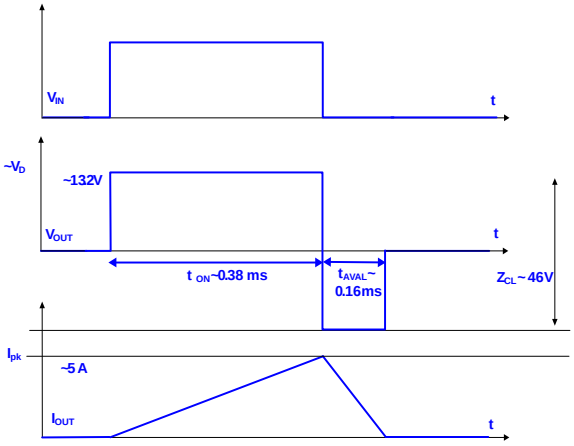

Figure 76. Idealized Wave−Set in a Hypothetical Inductive Switching Event− Calculating the Junction Temperature

The t_{ON} and t_{AVAL} are calculated as ~0.38 ms and ~0.16 ms using the equations below.

$$t_{ON} = \frac{L \cdot I_{pk}}{V_D - V_{DSON}} \quad \text{(eq. 19)}$$

$$t_{AVAL} = \frac{L \cdot I_{pk}}{|V_D - V_{ZCL}|} \quad \text{(eq. 20)}$$

The average power dissipations during the charging and the avalanche event can then be approximated as 2 Watts and 80 Watts respectively. These power levels have been calculated assuming an ideal straight line decay curve for the current during charge and discharge cycles. In a real application, the average power levels should rather be measured directly (most measuring equipment's can perform mathematical exercises to output measured powers) than performing these approximated calculations.

Now, referring to the set of curves in Figure 74, the x−axis defines the time period of the power pulse and the y−axis specs the thermal resistance for different duty cycle operations. Extrapolating the thermal resistance from the single pulse curve at ~ 0.38 ms (for the charge cycle) as ~ 1.2 °C/Watt, the temperature rise can be calculated as 1.2*2 ~ 2.4 °C. With a similar extrapolation for the discharge event, the temperature rise can be calculated as 0.8*80 ~ 64 °C. Adding this temperature rise to the ambient temperature, the junction temperature at the end of the SCIS event can be calculated as 25 + 2.4 + 64 ~ 92 °C.

In case of repetitive switching, the duty cycle curve should be referred to instead of the single pulse curve. For instance, if the inductance per Figure 76 is switched at a frequency of 100 Hz, the time period is calculated as 10 msec. The duty cycles for the charge and discharge event can then be calculated as 0.38/10 ~ 3.8% and 0.16/10 ~ 1.6% respectively. These curves can be interpolated for an estimated thermal resistance, and junction temperature can be calculated in a similar way as described above.

The calculation here assumes an averaged rectangular power profile equivalent for the inductive charge and discharge events which is not exactly accurate and may not necessarily be true in every application. The purpose of the above exercise was to demonstrate the interpretation and use of thermal resistance curves. In case the dynamic temperature change is of interest, the instantaneous power profile needs to be fed into a calculator that utilizes the foster R−C model (refer section Foster and Cauer Networks) and performs piece−wise integration using a set formulae to estimate the corresponding temperature profile. Such profiles can be provided on specific customer requests.

In all the aforementioned calculations and R−C networks, junction−to−ambient thermal resistance model has been shown. This is because of its greater relevance in practical scenarios. While a junction−to−case (or junction−to−pin) thermal resistance may seem like a convenient tool to estimate junction temperature by simply recording the case temperature during a power event, it could be misleading to use the published junction−to−case thermal resistance numbers. The premise behind a junction−to−case measurement is the assumption that the "case" of the device is treated as the "thermal ground", and should remain at a fixed known temperature regardless of dynamic changes in the junction temperature. Such a condition is difficult to achieve in practice, and nearly impossible over short transients where case temperature sways with the variations in dynamic power levels. Further, most temperature recording devices like thermocouples have response times way higher than typical power transients applied in automotive PWM applications, making it difficult to predict the exact case temperature. The junction−to−ambient counterpart, comparatively, is more reliable in the sense that ambient temperature can be controlled (through proper heat sinking and controlled air flow) more precisely in case of dynamic power changes.

Design Philosophy − Protection Features

The protection features in **onsemi** High Side SmartFETs, particularly − current limitation and temperature shutdown are designed taking into account the thermal performance of the device. While low power devices employ linear current limit with thermally driven retry strategy, high power devices realized on dense technologies use a more precise current limit peak detect turn off and a timer based retry strategy. From a layout standpoint, a thermal map of the die is simulated to assess the region's most sensitive (in terms of temperature changes) to the inflicted power. The temperature sense structures are laid out to optimize a) the maximum die temperature, b) linearity of sensors w.r.t max temperature on the die, and c) the required delta for differential temperature sensing to limit the transient thermal stresses. Placement of these sensors becomes further challenging in the devices that incorporate a clip covering the active source area. Layout for the current sense structures as well considers a uniform current density while avoiding constriction channels that could potentially create hotspots on the die. In addition to the layout, the analog control circuitry for these protection features also needs to be designed for the required thermal performance. The thresholds for control activation and the temperature coefficients of the circuit elements are primarily considered while designing this circuitry.

REFERENCES

1. https://chem.libretexts.org/Textbook_Maps/Inorganic_Chemistry_Textbook_Maps/Map%3A_Inorganic_Chemistry_(Wikibook)/Chapter_10%3A_Electronic_Properties_of_Materials%3A_Superconductors_and_Semiconductors/10.4_Semiconductors%3A_band_gaps%2C_colors%2C_conductivity_and_doping
2. Intusoft Newsletter, October 1988, pp 11−6 to 11−7, http://www.intusoft.com/nlpdf/nl11.pdf.
3. S. Ben−Yaakov, M.M. Peretz, B. Hesterman, "A SPICE compatible behavioral electrical model of a heated tungsten filament", Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, vol. 2, pp. 1079−1084, 2005.
4. http://www.aecouncil.com/Documents/AEC_Q100−012.pdf
5. https://www.iso.org/standard/50925.html

Table 4. GLOSSARY OF ABBREVIATIONS

#	Table	Description
1	DMOS	Double Diffused MOS
2	N−FET	N Channel Field Effect Transistor
3	CMOS	Complementary MOSFET pair
4	OEM	Original Equipment Manufacturer
5	Z_{VD}	Over−Voltage/ESD Clamp for the control section in a High Side Device
6	Z_{Sense}	Over−Voltage/ESD Clamp for the Current Sense Output
7	Z_{ESD}	ESD protection diodes for logic inputs
8	A/D	Analog to Digital Converter
9	I/O	Input/Output
10	RMS	Root Mean Square
11	ECU	Electronic Control Unit
12	PWM	Pulse Width Modulation
13	LED	Light Emitting Diode
14	RSC	Repetitive Short Circuit
15	SR	Sense Ratio
16	SR_{Err}	Error Factor in Sense Ratio
17	TSD	Temperature Shutdown
18	DTSD	Differential/Delta Thermal Shutdown
19	I_{OUT}	Output (Drain−Source) Current
20	CS	Current Sense Terminal
21	OUT	Output Terminal
22	V_{OFF}	Input Offset of CS op−amp
23	V_{th}	Threshold Voltage of Power FET
24	R_{LEAK}	Leakage Resistance during open load condition
25	I_{LOAD}	Current through the load− may differ from I_{OUT}
26	GND	Ground Terminal
27	V_{BATT}	Battery Voltage
28	$I_{L(OFF)}$	Off−State Output Leakage Current
29	V_D	Drain Voltage
30	V_{IN_HYST}	Input Hysteresis window
31	V_{IN}	Voltage at the input terminal
32	V_{SENSE}	Voltage at the Sense Terminal measured across the sense resistor, equivalent to ”V_{CS}”
33	I_{CS_REV}	Current through the CS pin in case of Reverse Battery Connection, equivalent to ”−I_{CS}”
34	R_{CS}	Sense Resistor to Ground
35	I_{REV}	Current through Body−Diode during reverse battery, equivalent to ”−I_{OUT}”
36	I_{LIM_SC1}/I_{LIM_Hi}	Current Limit − High
37	I_{LIM_SC2}/I_{LIM_Lo}	Fold Back Current Limit
38	I_{LIM}	Typical Current Limit
39	$R_{DS(ON)}$	Channel Resistance in ON State, equivalent to ”R_{ON}”
40	V_{CLAMP}/Z_{CL}	Over−Voltage Active Clamping Structure for SCIS events, equivalent to ”V_{OUT_CL}”
41	V_{DS_SAT}	Output Voltage Drop Limitation at Light Loads, equivalent to ”V_{DS_ON}”
42	I_{GND_REV}	Current through the GND pin in case of Reverse Battery Connection
43	Z_{GND}	Ground Impedance network comprised of resistor and diode in parallel

Table 4. GLOSSARY OF ABBREVIATIONS

#	Table	Description
44	R_{DEN}	Diagnosis Enable/Disable Resistance interfaced to microcontroller, equivalent to ”R_{CSE}”
45	t_{CS_High1}	CS_EN High to CS High delay time
46	t_{CS_Low1}	CS_EN Low to CS Low delay time
47	t_{CS_High2}	VIN High to CS High Delay Time
48	t_{CS_Low2}	VIN Low to CS Low Delay Time
49	t_{on}	VIN Rise to 90% VOUT
50	t_{off}	VIN Fall to 10% VOUT
51	t_{D_ON}	Turn−On Delay Time, to 10% VOUT, VD = ” ” V, RL = ” ” Ohms
52	t_{D_OFF}	Turn−Off Delay Time, to 90% VOUT, VD = ” ” V, RL = ” ” Ohms
53	tskew	Differential Pulse Skew
54	T_{TSD}	Thermal Shutdown Threshold
55	T_{TSD_HYS}	Thermal Shutdown Hysteresis
56	ΔT_{J_RST}	Delta Thermal Shutdown Hysteresis
57	V_{OV}	Over voltage Protection
58	R_{IN}	Input Resistance interfaced to microcontroller
59	DEN	Current Sense/Diagnostic Enable Terminal, equivalent to “CS_EN”
60	R_{CS}	Sense Resistor to Ground
61	R_{PU}	Pull up resistance for Off State Open Load Detection and Pull down resistance to detect Short Circuit Output to battery
62	S_{PU}	Switch to control R_{PU} connection to battery
63	$R_{A/D}$	Protects micro controller during over voltage and reverse polarity.
64	R_{GND}	Ground Resistance
65	Z_{CS}	ESD structure (internal) connected from VD to CS terminal.
66	SOA	Safe operating area
67	IGBTs	Insulated gate bipolar transistor
68	SCR	Silicion controlled rectifier
69	EMI	Electro magnetic interferance
70	$R_{PROTECT}$	Protection resistor for cluster load
71	t_{av}/t_{AVAL}	Avalanche time in an inductive discharge event
72	C_i	Capacitive ladder for thermal network
73	R_i	Resistance ladder for thermal network
74	τ_i	Time constant for a thermal network
75	$\theta_{Junction–Soldering\ Point}$	Junction to soldering point thermal resistance
76	$\theta_{Junction−Pin}$	Junction to pin thermal resistance
78	$\theta_{Junction−Case}$	Junction to case thermal resistance
79	EOL	End of life
80	K_{nom}/SR	Nominal current sense ratio
81	SC	Short circuit
82	$t_{cs\_Response}$	Current sense response time
83	V_{REF}	Reference voltage for comparator
84	DS	Diagnostic Select, equivalent to “CS_SEL”
85	C_{CS}	Capacitor for the current sense filter
86	$V_{(SENSE)\ SAT}$	Saturation voltage at CS pin
87	K_x	Constant accounting for device’s physical dimensions
88	α	Channel length modulation coefficient

Table 4. GLOSSARY OF ABBREVIATIONS

#	Table	Description
89	RCL	Repetitive clamp switching
90	I_{pk}	Peak current in SCIS event
91	L_{eff}	Effective inductance in a SCIS event
92	SCIS	Self−clamped inductive switching
93	V_{ZCL}	Breakdown voltage of the overvoltage protection clamps
94	V_{DSON}	On state potential drop
95	R_L	Load resistance
96	C_{DS}	Drain to source Capacitance
97	C_{GD}	Gate to drain Capacitance
98	C_{GS}	Gate to source capacitance
99	SR_{off}	Slew Rate during turn off
100	SR_{on}	Slew rate during turn on
101	V_{INH_MIN}	Minimum high level input voltage
102	V_{INL_MAX}	Maximum low level input voltage
103	R_{PD}	Pull down resistor for short circuit to detection
104	C_{OUT}	Output capacitor
105	Z_L	Load impedance
106	D_{GND}	Ground network diode
107	V_{GND}	Voltage across the ground resistor
108	V_{RIN}	Voltage across the input resistor
109	V_{OUT_MICRO}	Voltage at the logic output of the microcontroller
110	C_{SUPPLY}	Supply capacitor
111	V_{NOM}	Nominal rated bulb voltage
112	P_{NOM}	Nominal rated bulb power
113	$V_{ref\_deltaTj}$	Reference Voltage for DTSD comparator
114	V_{ref_Tjmax}	Reference voltage for DTSD comparator
115	I_{DEN_REV}	Reverse current through DEN terminal
116	I_{IN_REV}	Reverse current through input terminal
117	PCB	Printed circuit board
118	t_{Bulb_ON}	Time required to turn on the bulb
119	T_{REF}	Desired bulb filament temperature

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