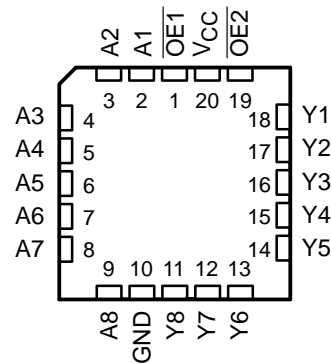- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **High-Impedance State During Power Up and Power Down**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Power Off Disables Inputs/Outputs, Permitting Live Insertion**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs**

**SN54LVTH541 . . . J OR W PACKAGE**
**SN74LVTH541 . . . DB, DGV, DW, OR PW PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{OE1}$ | 1 | 20 | $V_{CC}$ |
| A1 | 2 | 19 | $\overline{OE2}$ |
| A2 | 3 | 18 | Y1 |
| A3 | 4 | 17 | Y2 |
| A4 | 5 | 16 | Y3 |
| A5 | 6 | 15 | Y4 |
| A6 | 7 | 14 | Y5 |
| A7 | 8 | 13 | Y6 |
| A8 | 9 | 12 | Y7 |
| GND | 10 | 11 | Y8 |
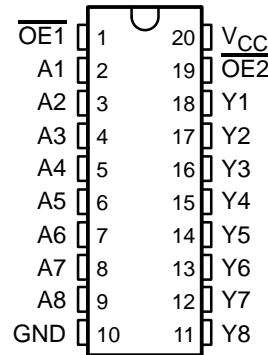
**SN54LVTH541 . . . FK PACKAGE**
**(TOP VIEW)**

Pins (top): A2 (3), A1 (2), $\overline{OE1}$ (1), $V_{CC}$ (20), $\overline{OE2}$ (19)
Left side: A3 (4), A4 (5), A5 (6), A6 (7), A7 (8)
Right side: Y1 (18), Y2 (17), Y3 (16), Y4 (15), Y5 (14)
Bottom: A8 (9), GND (10), Y8 (11), Y7 (12), Y6 (13)

## description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH541 are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When $V_{CC}$ is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH541 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH541 is characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TEXAS INSTRUMENTS**

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
| --- | --- | --- | --- |
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

## logic symbol[†]
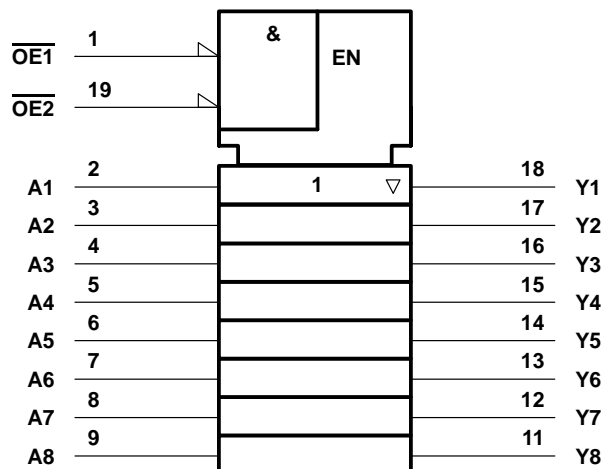


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



**To Seven Other Channels**

TEXAS
INSTRUMENTS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ............................................................. –0.5 V to 4.6 V

Input voltage range, $V_I$ (see Note 1) ................................................. –0.5 V to 7 V

Voltage range applied to any output in the high-impedance or power-off state, $V_O$
  (see Note 1) ........................................................................ –0.5 V to 7 V

Current into any output in the low state, $I_O$: SN54LVTH541 ..................................... 96 mA
                                              SN74LVTH541 ..................................... 128 mA

Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH541 ....................... 48 mA
                                                             SN74LVTH541 ....................... 64 mA

Input clamp current, $I_{IK}$ ($V_I < 0$) ................................................. –50 mA

Output clamp current, $I_{OK}$ ($V_O < 0$) ............................................... –50 mA

Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package ................................ 115°C/W
                                                     DGV package ................................ 146°C/W
                                                     DW package ................................. 97°C/W
                                                     PW package ................................. 128°C/W

Storage temperature range, $T_{stg}$ ............................................... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
  functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
  implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
        3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

|  |  | SN54LVTH541 | | SN74LVTH541 | | UNIT |
|---|---|---|---|---|---|---|
|  |  | MIN | MAX | MIN | MAX |  |
| $V_{CC}$ | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | 2 |  | 2 |  | V |
| $V_{IL}$ | Low-level input voltage |  | 0.8 |  | 0.8 | V |
| $V_I$ | Input voltage |  | 5.5 |  | 5.5 | V |
| $I_{OH}$ | High-level output current |  | –24 |  | –32 | mA |
| $I_{OL}$ | Low-level output current |  | 48 |  | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |  | 10 |  | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 |  | 200 |  | µs/V |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH541 MIN | TYP† | MAX | SN74LVTH541 MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = −18 mA | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 2.7 V to 3.6 V, | $I_{OH}$ = −100 µA | $V_{CC}$−0.2 | | | $V_{CC}$−0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = −8 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = −24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = −32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | | | 10 | | | 10 | µA |
| | Control inputs | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | |
| | Data inputs‡ | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | −5 | | | −5 | |
| $I_{off}$ | | $V_{CC}$ = 0, $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | | ±100 | µA |
| $I_{I(hold)}$ | Data inputs | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| | | | $V_I$ = 2 V | −75 | | | −75 | | | |
| $I_{OZH}$ | | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 5 | | | 5 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | −5 | | | −5 | µA |
| $I_{OZPU}$§ | | $V_{CC}$ = 0 to 1.5 V, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = Don't care | | | | ±100 | | | ±100 | µA |
| $I_{OZPD}$§ | | $V_{CC}$ = 1.5 V to 0, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = Don't care | | | | ±100 | | | ±100 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 0.19 | | | 0.19 | mA |
| | | | Outputs low | | | 5 | | | 5 | |
| | | | Outputs disabled | | | 0.19 | | | 0.19 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ − 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | | 3 | | | 3 | pF |
| $C_O$ | | $V_O$ = 3 V or 0 | | | | 7 | | | 7 | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ Unused pins at $V_{CC}$ or GND.
§ This parameter is warranted but not production tested.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C$_L$ = 50 pF (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH541 V$_{CC}$ = 3.3 V ± 0.3 V | | SN54LVTH541 V$_{CC}$ = 2.7 V | | SN74LVTH541 V$_{CC}$ = 3.3 V ± 0.3 V | | | SN74LVTH541 V$_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | MAX | |
| t$_{PLH}$ | A | Y | 1 | 3.7 | | 4 | 1.1 | 2.4 | 3.5 | | 3.9 | ns |
| t$_{PHL}$ | | | 1 | 3.7 | | 4 | 1.1 | 2.4 | 3.5 | | 3.9 | |
| t$_{PZH}$ | $\overline{OE}$ | Y | 1.4 | 5.3 | | 6.3 | 1.5 | 3.5 | 5.2 | | 6.2 | ns |
| t$_{PZL}$ | | | 1.4 | 5.4 | | 6 | 1.5 | 3.7 | 5.3 | | 5.9 | |
| t$_{PHZ}$ | $\overline{OE}$ | Y | 1.4 | 5.8 | | 6.1 | 1.5 | 3.9 | 5.6 | | 5.9 | ns |
| t$_{PLZ}$ | | | 1.4 | 5.4 | | 5.7 | 1.5 | 3 | 5 | | 5.3 | |

† All typical values are at V$_{CC}$ = 3.3 V, T$_A$ = 25°C.

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## PARAMETER MEASUREMENT INFORMATION
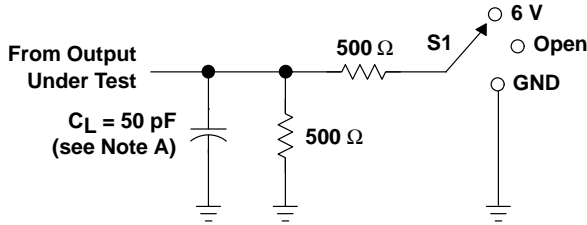


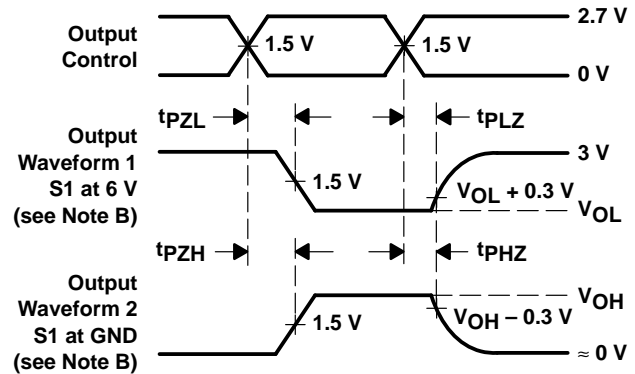| TEST | S1 |
|------|-----|
| $t_{pd}$ | Open |
| $t_{PLZ}$/$t_{PZL}$ | 6 V |
| $t_{PHZ}$/$t_{PZH}$ | GND |

**LOAD CIRCUIT**
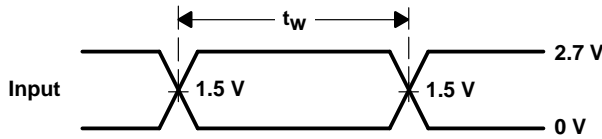
**VOLTAGE WAVEFORMS**
**PULSE DURATION**
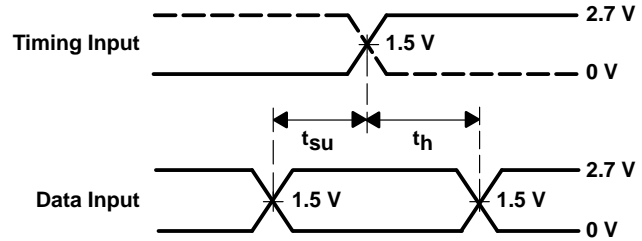
**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**
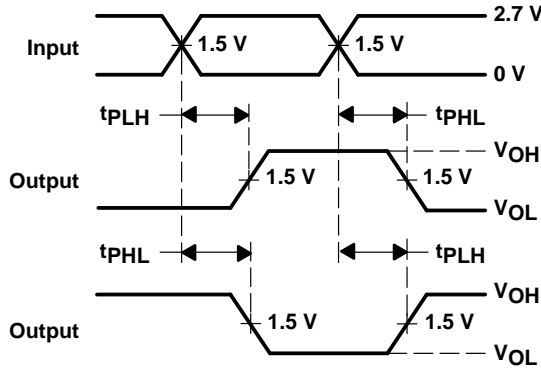
**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**
**LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

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