4.3mΩ, 100V, N-Channel Power MOSFET SRT10N043H

General Description

The Sanrise SRT10N043H is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N043H break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N043H is available in PDFN5*6 and TO-220C and TO-263-2 packages.

Features

- Ultra Low

$R_{DS(ON)\_TYP}$ = 3.7mΩ ,PDFN5*6 @V_{GS} = 10V.

$R_{DS(ON)\_TYP}$ = 4.1mΩ ,TO-220C @V_{GS} = 10V.

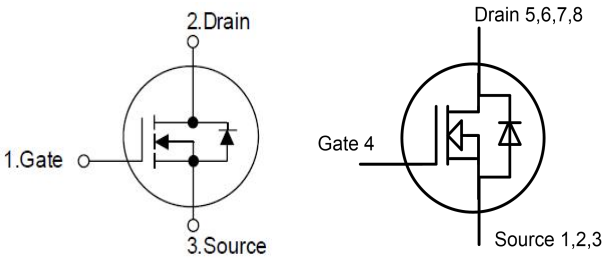
$R_{DS(ON)\_TYP}$ = 3.9mΩ ,TO-263-2 @V_{GS} = 10V.

- Ultra Low Gate Charge, Qg=57nC typ.
- Fast switching capability
- Robust design with better EAS performance

Application

- Server/Telecom
- High Power Supply
- E-Tools
- BMS

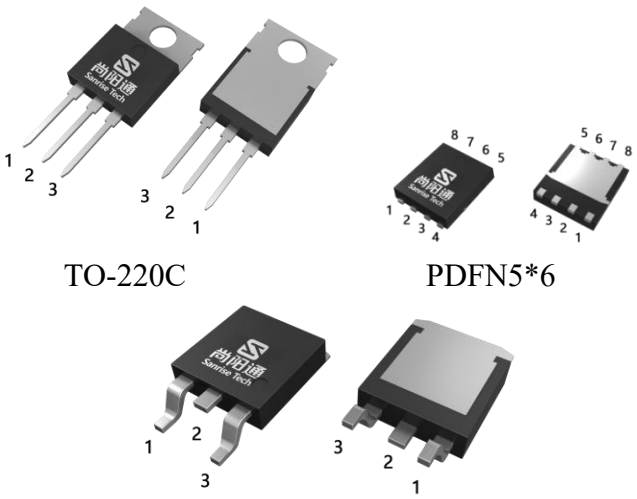
Symbol



TO-220C,TO-263-2 PDFN5*6

Figure 1 Symbol of SRT10N043H

Package Type



TO-220C PDFN5*6

TO-263-2

Figure 2 Package Type of SRT10N043H

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Ordering Information

SRT10N043H□□–□

Circuit Type

Package
D56: PDFN5*6
TC: TO-220C
S2: TO-263-2

E: Lead Free
G: Green

Blank: Tube
TR: Tape & Reel

Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT10N043HD56TR-G	SRT10N043HD56G	Tape & Reel
TO-220C	SRT10N043HTC-E	SRT10N043HTCE	Tube
TO-263-2	SRT10N043HS2TR-E	SRT10N043HS2E	Tape & Reel

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Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	100		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current	T_C=25ºC	I_D	PDFN5*6	125	A
			TO-220C	125	
			TO-263-2	125	
	T_C=100ºC		PDFN5*6	77	
			TO-220C	79	
			TO-263-2	81	
Pulsed Drain Current (Note 2)		I_{DM}	PDFN5*6	500	A
			TO-220C	500	
			TO-263-2	500	
Max Power Dissipation		P_D	119		W
Avalanche Destructive Energy, Single Pulse (Note 4)		E_{AS_Limit}	625		mJ
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	110		mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.2		mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	40.0		A
Continuous Diode Forward Current		I_S	100		A
Diode Pulse Current		$I_{S.PULSE}$	300		A
Operating Junction Temperature		T_J	150		ºC
Storage Temperature		T_{STG}	-55 to 150		ºC
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260		ºC

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. I_{AS}= 21.0A, V_{DD}= 50V, R_G= 25Ω, Starting T_J= 25°C
4. I_{AS_Limit}= 50A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

Thermal Resistance

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance， Junction-to-Case	PDFN5*6	R_{thJC}			1.05	ºC/W
	TO-220C				0.94	
	TO-263-2				0.94	
Thermal Resistance， Junction-to-Ambient	PDFN5*6	R_{thJA}			50	
	TO-220C				60	
	TO-263-2				60	

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Electrical Characteristics

T_J = 25℃, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250uA	100			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=100V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	PDFN5*6	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		3.7	4.3	mΩ
	TO-220C				4.1	4.5	
	TO-263-2				3.9	4.3	
Gate Resistance		R_G	f=1MHz, Open Drain		1.0		Ω
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS}=50V, V_{GS}=0V, f=1MHz		3.9		nF
Output Capacitance		C_{OSS}			1.3		nF
Reverse Transfer Capacitance		C_{RSS}			24		pF
Effective output capacitance, energy related NOTE5		$C_{O(er)}$	V_{GS}=0V, V_{DS}=0…60V		1.7		nF
Effective output capacitance, time related NOTE6		$C_{O(tr)}$			2.1		
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=50V, I_D=20A R_G=3.0Ω, V_{GS}=10V		14		nS
Rise Time		t_r			7		
Turn-off Delay Time		$t_{d(off)}$			32		
Fall Time		t_f			11		
Gate Charge Characteristics							
Gate to Source Charge		Q_{gs}	V_{DD}=50V, I_D=20A V_{GS}=0 to 10V		16		nC
Gate to Drain Charge		Q_{gd}			11		
Gate Charge Total		Q_g			57		
Gate Plateau Voltage		$V_{plateau}$			4.2		V
Gate Charge Total, sync FET		Q_g	V_{DD}=0.1V, V_{GS}=0 to 10V		49		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_{SD}=20A		0.81	1.0	V
Reverse Recovery Time		t_{rr}	V_R=50V, I_F=20A dI$_F$/dt=100A/us		50		nS
Reverse Recovery Charge		Q_{rr}			75		nC
Peak Reverse Recovery Current		I_{rrm}			3		A

Note:

5. $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 60V

6. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 60 V

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Sanrise Technology Limited Company

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