

## General Description

The Sanrise SRT15N110H is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT15N110H break down voltage is 150V and it has a high rugged avalanche characteristics. The SRT15N110H is available in PDFN5\*6 and TO-220C packages.

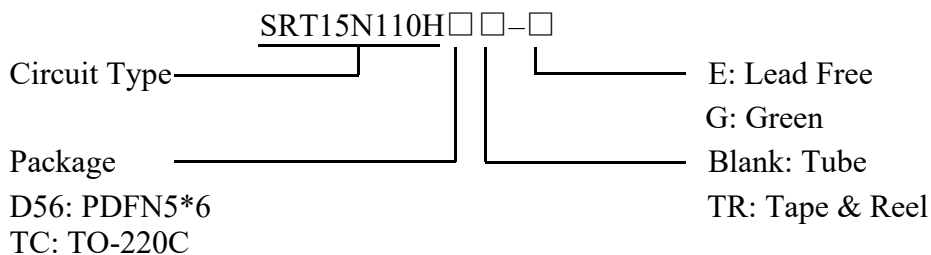
## Features

- Ultra Low  
 $R_{DS(ON\_TYP)} = 9.1m\Omega$ , PDFN5\*6 @ $V_{GS} = 10V$ .  
 $R_{DS(ON\_TYP)} = 10.3m\Omega$ , TO-220C @ $V_{GS} = 10V$ .
- Ultra Low Gate Charge,  $Q_g=40nC$  typ.
- Fast switching capability
- Robust design with better EAS performance
- EMI Improved
- Non-automotive Qualified

## Application

- Server/Telecom
- High Power Supply
- Solar
- UPS

## Ordering Information



Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT15N110HD56TR-G	SRT15N110HD56G	Tape & Reel
TO-220C	SRT15N110HTC-G	SRT15N110HTCG	Tube

## Symbol

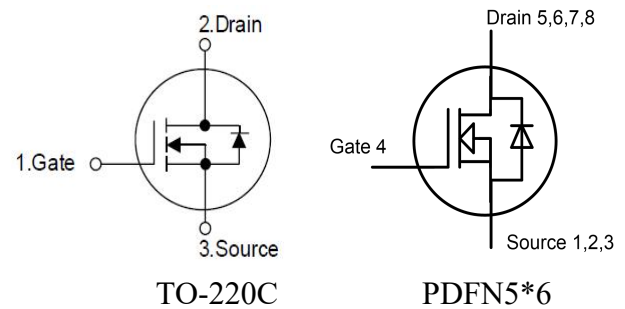


Figure 1 Symbol of SRT15N110H

## Package Type

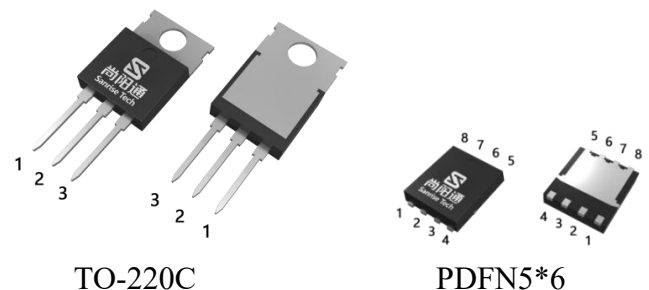


Figure 2 Package Type of SRT15N110H

**11mΩ, 150V, N-Channel Power MOSFET**
**SRT15N110H**
**Absolute Maximum Ratings**

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		$V_{DSS}$	150		V
Gate-Source Voltage		$V_{GSS}$	±20		V
Continuous Drain Current, Package Limited	$T_C=25^{\circ}C$	$I_D$	PDFN5*6	80	A
	$T_C=100^{\circ}C$		TO-220C	78.5	
$T_C=25^{\circ}C$			PDFN5*6	56	
	TO-220C		55.5		
Continuous Drain Current, Silicon	$T_C=25^{\circ}C$		PDFN5*6	80	
			TO-220C	78.5	
Pulsed Drain Current (Note 2)		$I_{DM}$	PDFN5*6	320	
			TO-220C	314	
Power Dissipation ( $T_C = 25^{\circ}C$ )		$P_D$	157		W
Avalanche Destructive Energy, Single Pulse (Note 4)		$E_{AS\_Limit}$	370		mJ
Avalanche Energy, Single Pulse (Note 3)		$E_{AS}$	81		mJ
Avalanche Energy, Repetitive (Note 2)		$E_{AR}$	0.1		mJ
Avalanche Current, Repetitive (Note 2)		$I_{AR}$	16		A
Continuous Diode Forward Current		$I_S$	80		A
Diode Pulse Current		$I_{S\_PULSE}$	320		A
Operating Junction Temperature		$T_J$	175		$^{\circ}C$
Storage Temperature		$T_{STG}$	-55 to 175		$^{\circ}C$
Lead Temperature (Soldering, 10 sec)		$T_{LEAD}$	260		$^{\circ}C$

Note:

- Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
- Repetitive Rating: Pulse width limited by maximum junction temperature
- $I_{AS} = 18A$ ,  $V_{DD} = 60V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}C$
- $I_{AS\_Limit} = 38.5A$ ,  $V_{DD} = 60V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}C$

**Thermal Resistance**

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	PDFN5*6	$R_{thJC}$			0.95	$^{\circ}C/W$
	TO-220C				0.95	
Thermal Resistance, Junction-to-Ambient	PDFN5*6	$R_{thJA}$			50	
	TO-220C				62	

**11mΩ, 150V, N-Channel Power MOSFET**
**SRT15N110H**
**Electrical Characteristics**
 $T_J = 25^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Statistic Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	150			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=150V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	Forward	$V_{GS}=20V, V_{DS}=0V$			100	nA
	Reverse	$V_{GS}=-20V, V_{DS}=0V$			-100	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=0.25mA$	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	PDFN5*6	$V_{GS}=10V, I_D=60A$		9.1	11	mΩ
	TO-220C			10.3	12.8	
Gate Resistance	$R_G$	$f=1MHz, \text{Open Drain}$		1.1		Ω
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=50V, V_{GS}=0V, f=1MHz$		2.25		nF
Output Capacitance	$C_{OSS}$			1.03		nF
Reverse Transfer Capacitance	$C_{RSS}$			18		pF
Effective output capacitance, energy related <small>NOTE5</small>	$C_{O(er)}$	$V_{GS}=0V, V_{DS}=0\dots 90V$		28		nF
Effective output capacitance, time related <small>NOTE6</small>	$C_{O(tr)}$			0.9		
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=75V, I_D=60A, R_G=1.6\Omega, V_{GS}=10V$		9		nS
Rise Time	$t_r$			3		
Turn-off Delay Time	$t_{d(off)}$			15		
Fall Time	$t_f$			3		
<b>Gate Charge Characteristics</b>						
Gate to Source Charge	$Q_{gs}$	$V_{DD}=75V, I_D=60A, V_{GS}=0 \text{ to } 10V$		12.8		nC
Gate to Drain Charge	$Q_{gd}$			9.4		
Gate Charge Total	$Q_g$			40		
Gate Plateau Voltage	$V_{plateau}$			4.9		V
Gate Charge Total, sync FET	$Q_g$	$V_{DD}=0.1V, V_{GS}=0 \text{ to } 10V$		33.4		nC
<b>Reverse Diode Characteristics</b>						
Drain-Source Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_{SD}=60A$		0.87	1.1	V
Reverse Recovery Time	$t_{rr}$	$V_R=75V, I_F=60A, dI_F/dt=100A/\mu s$		16		nS
Reverse Recovery Charge	$Q_{rr}$			15		nC
Peak Reverse Recovery Current	$I_{rrm}$			1.2		A

Note:

- $C_{O(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 90V
- $C_{O(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 90 V



Sanrise Technology Limited Company

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#### **Main Site:**

##### **- Headquarter**

Shenzhen Sanrise Technology Co., LTD.  
A1206, Skyworth building, No. 008, gaoxinnan 1st Road,  
Gaoxin District, Yuehai street,, Nanshan District, ShenZhen,  
P.R.China  
Tel: +86-755-22953335  
Fax: +86-755-22916878

##### **- Shanghai Office**

Sanrise Technology Limited Company  
Rm.401, Building B, No. 666, Zhangheng Road,  
Zhangjiang Hi-Tech Park, Shanghai, P.R.China  
Tel: +86-21-68825918