9mΩ, 100V, N-Channel Power MOSFET SRT10N090L

General Description

The Sanrise SRT10N090L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N090L break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N090L is available in PDFN5*6 and TO-252 and TO-220C and SOP-8 packages.

Features

- Ultra Low

$R_{DS(ON)\_TYP}$ = 7.6mΩ ,PDFN5*6 @V_{GS} = 10V.

$R_{DS(ON)\_TYP}$ = 7.8mΩ ,TO-252 @V_{GS} = 10V.

$R_{DS(ON)\_TYP}$ = 7.8mΩ ,TO-220C @V_{GS} = 10V.

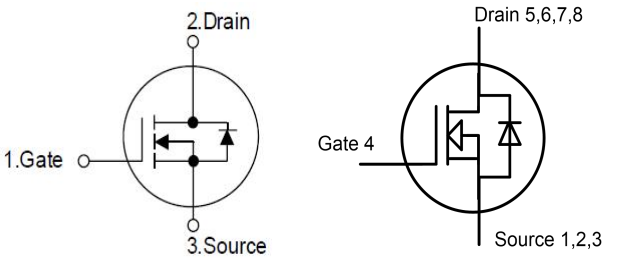
$R_{DS(ON)\_TYP}$ = 8.0mΩ ,SOP-8 @V_{GS} = 10V.

- Ultra Low Gate Charge, Qg=28.5nC typ.
- Fast switching capability
- Robust design with better EAS performance
- Non-automotive Qualified

Application

- Charger / Adapter
- Server/Telecom
- High Power Supply
- E-Tools

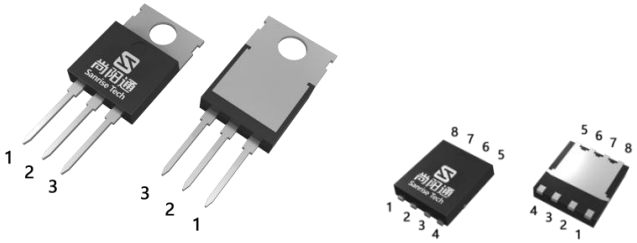
Symbol



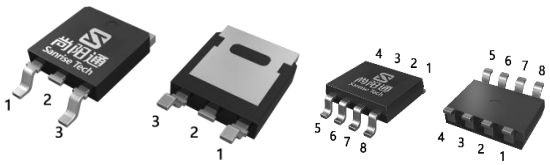
TO-220C,TO-252 PDFN5*6，SOP-8

Figure 1 Symbol of SRT10N090L

Package Type



TO-220C PDFN5*6



TO-252 SOP-8

Figure 2 Package Type of SRT10N090L

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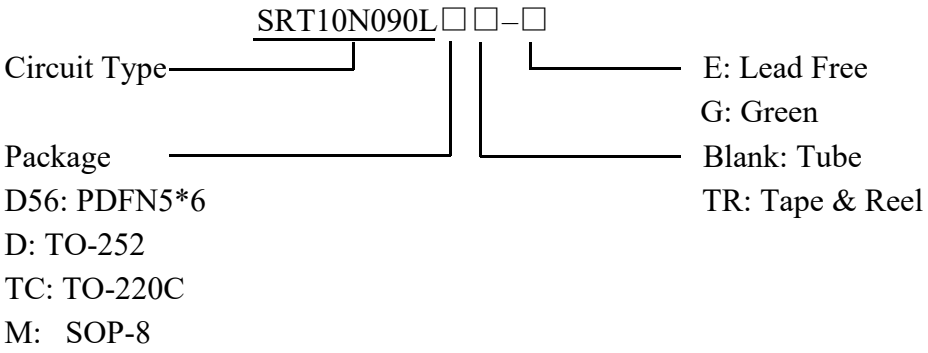
Ordering Information



Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT10N090LD56TR-G	SRT10N090LD56G	Tape & Reel
TO-252	SRT10N090LDTR-G	SRT10N090LDG	Tape &Reel
TO-220C	SRT10N090LTC-E	SRT10N090LTCE	Tube
SOP-8	SRT10N090LMTR-G	10N090LMG	Tape &Reel

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Absolute Maximum Ratings

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	100		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current	T_C=25ºC	I_D	PDFN5*6	65	A
			TO-252	68	
			TO-220C	68	
			SOP-8	17.5	
	T_C=100ºC		PDFN5*6	41	
			TO-252	43	
			TO-220C	43	
			SOP-8	11	
Pulsed Drain Current (Note 2)		I_{DM}	195		A
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	60		mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.1		mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	15		A
Continuous Diode Forward Current		I_S	65		A
Diode Pulse Current		$I_{S.PULSE}$	195		A
Operating Junction Temperature		T_J	150		ºC
Storage Temperature		T_{STG}	-55 to 150		ºC
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260		ºC

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. I_{AS}= 15.0A, V_{DD}= 50V, R_G= 25Ω, Starting T_J= 25°C

Thermal Resistance

Parameter		Symbol	Min	Typ	Max	Unit
Thermal Resistance，Junction-to-Case	PDFN5*6	R_{thJC}			1.7	ºC/W
Thermal Resistance，Junction-to-Ambient		R_{thJA}			50	ºC/W
Thermal Resistance，Junction-to-Case	TO-252	R_{thJC}			1.55	ºC/W
Thermal Resistance，Junction-to-Ambient		R_{thJA}			62	ºC/W
Thermal Resistance，Junction-to-Case	TO-220C	R_{thJC}			1.55	ºC/W
Thermal Resistance，Junction-to-Ambient		R_{thJA}			62	ºC/W
Thermal Resistance，Junction-to-Lead	SOP8	R_{thJL}			25	ºC/W
Thermal Resistance，Junction-to-Ambient	SOP8	R_{thJA}			80	ºC/W

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Electrical Characteristics

T_J = 25℃, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250uA	100			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=100V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.2	1.8	2.4	V
Static Drain-Source On-Resistance	PDFN5*6	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=10A		10.5	13.8	mΩ
	TO-252				10.7	14.0	
	TO-220C				10.7	14.0	
	SOP-8				10.7	14.0	
	PDFN5*6		V_{GS}=10V, I_D=20A		7.6	9.0	mΩ
	TO-252				7.8	9.0	
	TO-220C				7.8	9.0	
	SOP-8				8.0	9.0	
Gate Resistance		R_G	f=1MHz, Open Drain		1.2		Ω
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS}=50V, V_{GS}=0V, f=1MHz		1.8		nF
Output Capacitance		C_{OSS}			530		pF
Reverse Transfer Capacitance		C_{RSS}			10		pF
Effective output capacitance, energy related NOTE5		$C_{O(er)}$	V_{GS}=0V, V_{DS}=0…60V		720		pF
Effective output capacitance, time related NOTE6		$C_{O(tr)}$			850		
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=50V, I_D=20A R_G=3.0Ω, V_{GS}=10V		5.9		nS
Rise Time		t_r			4.3		
Turn-off Delay Time		$t_{d(off)}$			19.1		
Fall Time		t_f			6.0		
Gate Charge Characteristics							
Gate to Source Charge		Q_{gs}	V_{DD}=50V, I_D=20A V_{GS}=0 to 4.5V		6.2		nC
Gate to Drain Charge		Q_{gd}			5.0		
Gate Charge Total		Q_g			14.2		
Gate Charge Total		Q_g	V_{DD}=50V, I_D=20A,V_{GS}=0 to 10V		28.5		nC
Gate Charge Total, sync FET		Q_g	V_{DD}=0.1V, V_{GS}=0 to 10V		25.3		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_{SD}=20A		0.85	1.1	V
Reverse Recovery Time		t_{rr}	V_R=50V, I_F=20A dI$_F$/dt=100A/us		33		nS
Reverse Recovery Charge		Q_{rr}			41		nC
Peak Reverse Recovery Current		I_{rrm}			2.5		A

Note:5. CO(er) is a fixed capacitance that gives the same stored energy as COSS while VDS is rising from 0 to 60V

6. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 60 V

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Sanrise Technology Limited Company

http://www.sanrise-tech.com

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