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DATA SHEET
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ECOSPARK® Ignition IGBT

300 mJ, 400 V, N−Channel Ignition IGBT

ISL9V3040x3ST-F085C

Features

- SCIS Energy = 300 mJ at T_J = 25°C
- Logic Level Gate Drive
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

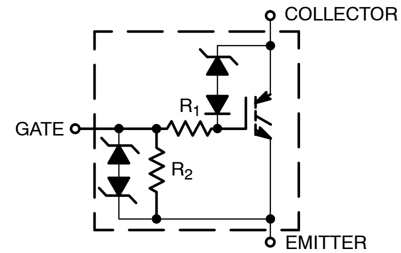
- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Application

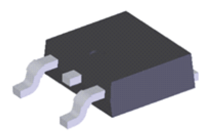
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage (IC = 1 mA)	400	V
BV_{ECS}	Emitter to Collector Voltage − Reverse Battery Condition (IC = 10 mA)	24	V
E_{SCIS25}	ISCIS = 14.2 A, L = 3.0 mHy, RGE = 1 KΩ, T_C = 25°C (Note 1)	300	mJ
$E_{SCIS150}$	ISCIS = 10.6 A, L = 3.0 mHy, RGE = 1 KΩ, T_C = 150°C (Note 2)	170	mJ
IC25	Collector Current Continuous at VGE = 4.0 V, T_C = 25°C	21	A
IC110	Collector Current Continuous at VGE = 4.0 V, T_C = 110°C	17	A
V_{GEM}	Gate to Emitter Voltage Continuous	±10	V
PD	Power Dissipation Total, T_C = 25°C	150	W
	Power Dissipation Derating, T_C > 25°C	1	W/°C
T_J, T_{STG}	Operating Junction and Storage Temperature	−55 to +175	°C
T_L	Lead Temperature for Soldering Purposes (1/8” from case for 10 s)	300	°C
T_{PKG}	Reflow Soldering according to JESD020C	260	°C
ESD	HBM−Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV
	CDM−Electrostatic Discharge Voltage at 1 Ω	2	kV

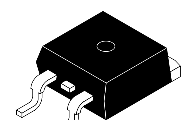
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self clamped inductive Switching Energy (ESCIS25) of 300 mJ is based on the test conditions that is starting T_J = 25°C, L = 3 mHy, ISCIS = 14.2 A, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.
2. Self Clamped inductive Switching Energy (ESCIS150) of 170 mJ is based on the test conditions that is starting T_J = 150°C, L = 3mHy, ISCIS = 10.6 A, VCC = 100 V during inductor charging and VCC = 0 V during time in clamp.

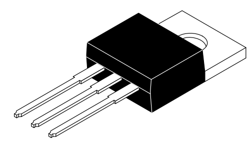




DPAK3
CASE 369AS

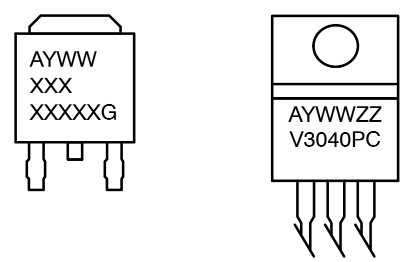


D2PAK−3
CASE 418AJ



TO−220−3LD
CASE 340AT

MARKING DIAGRAMS



A	=	Assembly Location
Y	=	Year
WW	=	Work Week
XXXX	=	Device Code
G	=	Pb−Free Package
ZZ	=	Assembly Lot Number
V3040PC	=	Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

November, 2021 − Rev. 2
Publication Order Number:
ISL9V3040−F085C/D

THERMAL RESISTANCE RATINGS

Characteristic	Symbol	Max	Units
Junction−to−Case – Steady State (Drain)	$R_{\theta JC}$	1	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Typ.	Max.	Units
OFF CHARACTERISTICS							
BV_{CER}	Collector to Emitter Breakdown Voltage	I_{CE} = 2 mA, V_{GE} = 0 V, R_{GE} = 1 kΩ, T_J = −40 to 150°C		370	400	430	V
BV_{CES}	Collector to Emitter Breakdown Voltage	I_{CE} = 10 mA, V_{GE} = 0 V, R_{GE} = 0, T_J = −40 to 150°C		390	420	450	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_{CE} = −75 mA, V_{GE} = 0 V, T_J = 25°C		30	–	–	V
BV_{GES}	Gate to Emitter Breakdown Voltage	I_{GES} = ±2 mA		±12	±14	–	V
I_{CER}	Collector to Emitter Leakage Current	V_{CE} = 175 V, R_{GE} = 1 kΩ	T_J = 25°C	–	–	25	µA
			T_J = 150°C	–	–	1	mA
I_{ECS}	Emitter to Collector Leakage Current	V_{EC} = 24 V	T_J = 25°C	–	–	1	mA
			T_J = 150°C	–	–	40	
R_1	Series Gate Resistance			–	70	–	Ω
R_2	Gate to Emitter Resistance			10K	–	26K	Ω
ON CHARACTERISTICS							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 6 A, V_{GE} = 4 V, T_J = 25°C		–	1.25	1.65	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 10 A, V_{GE} = 4.5 V, T_J = 150°C		–	1.58	1.80	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 15 A, V_{GE} = 4.5 V, T_J = 150°C		–	1.90	2.20	V
DYNAMIC CHARACTERISTICS							
$Q_{G(ON)}$	Gate Charge	I_{CE} = 10 A, V_{CE} = 12 V, V_{GE} = 5 V		–	17	–	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_{CE} = 1 mA, V_{CE} = V_{GE}	T_J = 25°C	1.3	–	2.2	V
			T_J = 150°C	0.75	–	1.8	
V_{GEP}	Gate to Emitter Plateau Voltage	V_{CE} = 12 V, I_{CE} = 10 A		–	3.0	–	V
SWITCHING CHARACTERISTICS							
$td_{(ON)R}$	Current Turn−On Delay Time−Resistive	V_{CE} = 14 V, R_L = 1 Ω, V_{GE} = 5 V, R_G = 470 Ω, T_J = 25°C		–	0.7	4	µs
t_{rR}	Current Rise Time−Resistive			–	2.1	7	
$td_{(OFF)L}$	Current Turn−Off Delay Time−Inductive	V_{CE} = 300 V, L = 1 mH, V_{GE} = 5 V, R_G = 470 Ω, I_{CE} = 6.5 A, T_J = 25°C		–	4.8	15	
t_{fL}	Current Fall Time−Inductive			–	2.8	15	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

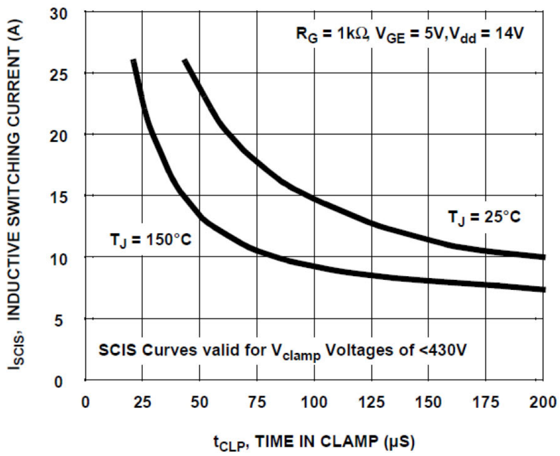


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

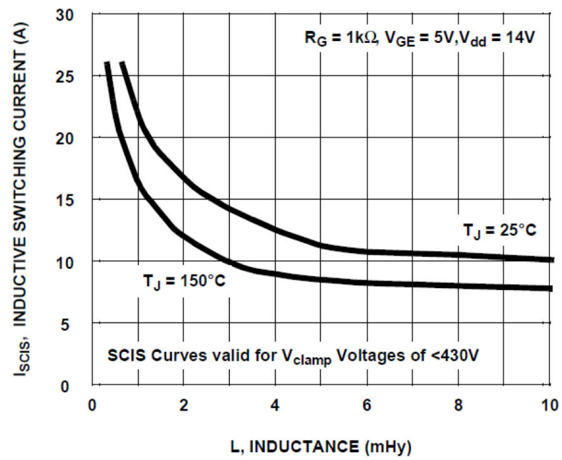


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

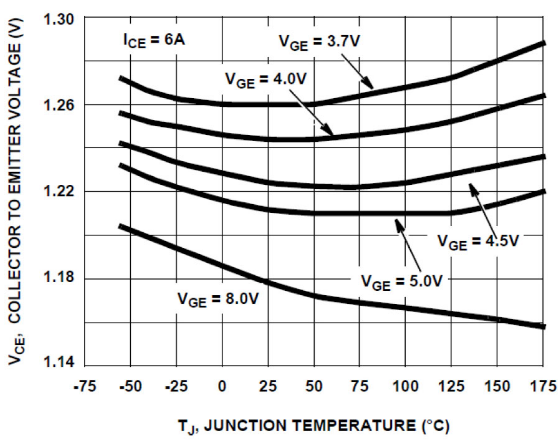


Figure 3. Collector to Emitter On−State Voltage vs. Junction Temperature

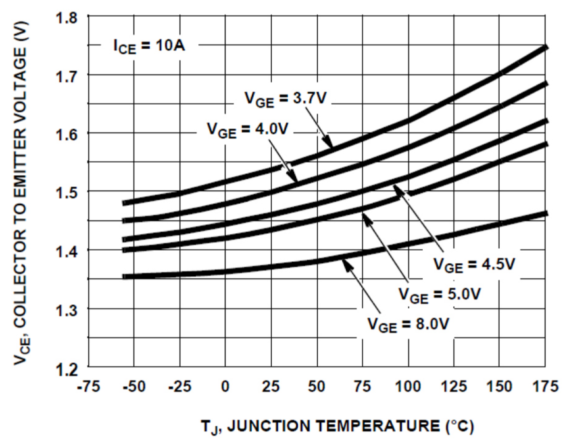


Figure 4. Collector to Emitter On−State Voltage vs. Junction Temperature

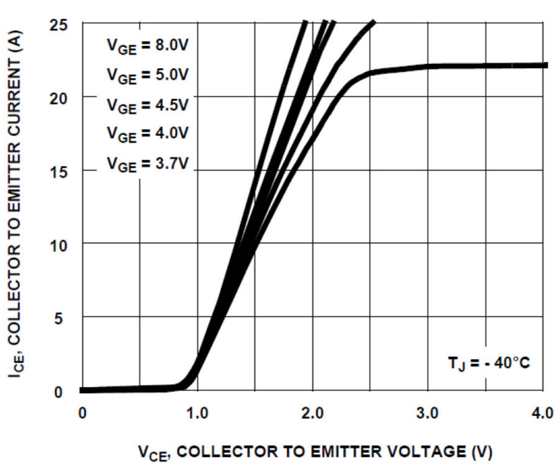


Figure 5. Collector to Emitter On−State Voltage vs. Collector Current

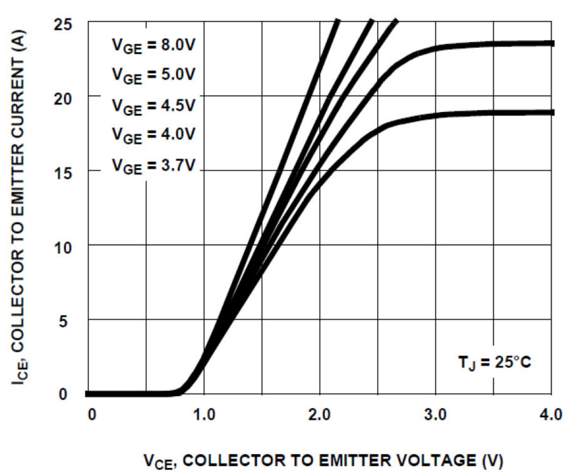


Figure 6. Collector to Emitter On−State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS (continued)

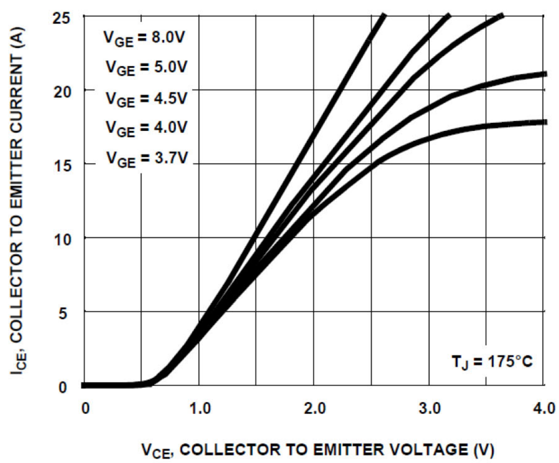


Figure 7. Collector to Emitter On−State Voltage vs. Collector Current

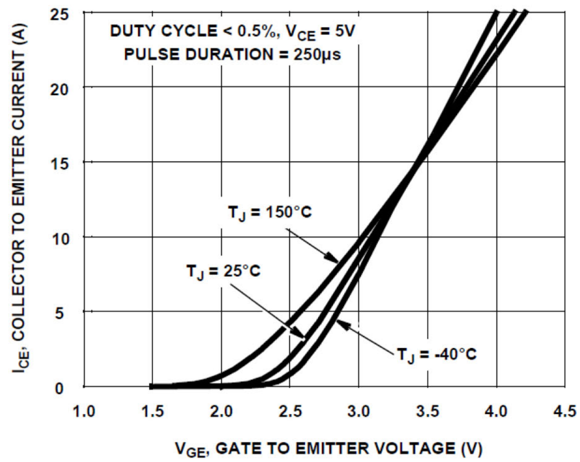


Figure 8. Transfer Characteristics

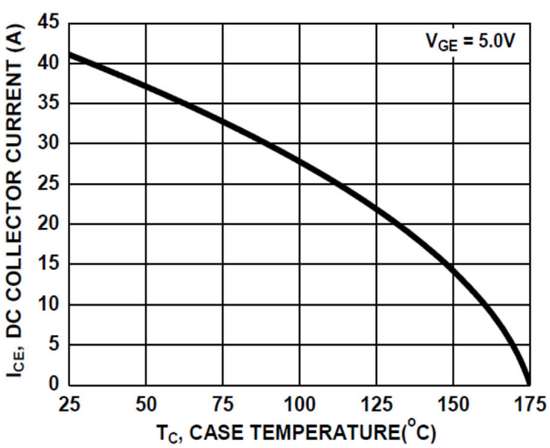


Figure 9. DC Collector Current vs. Case Temperature

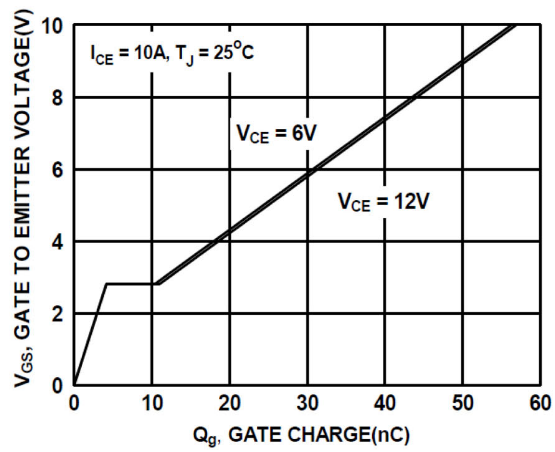


Figure 10. Gate Charge

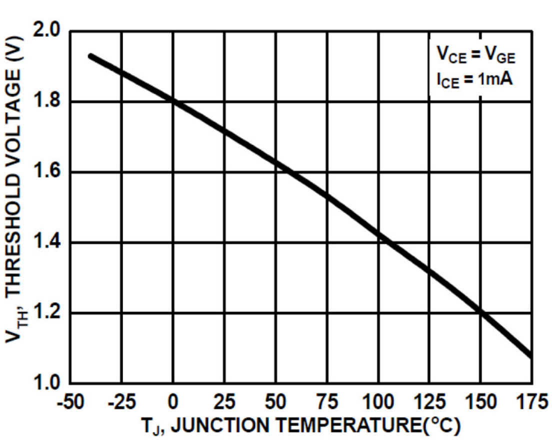


Figure 11. Threshold Voltage vs. Junction Temperature

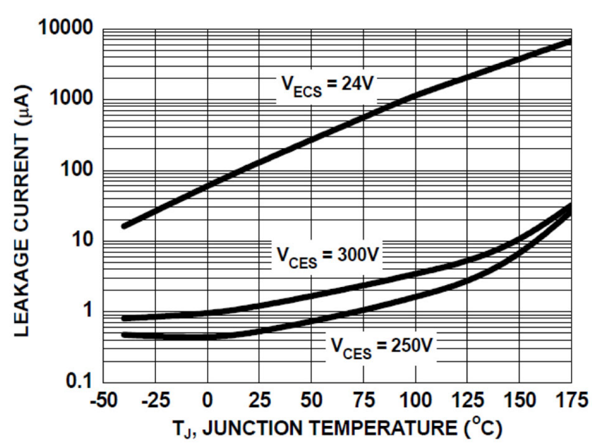


Figure 12. Leakage Current vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

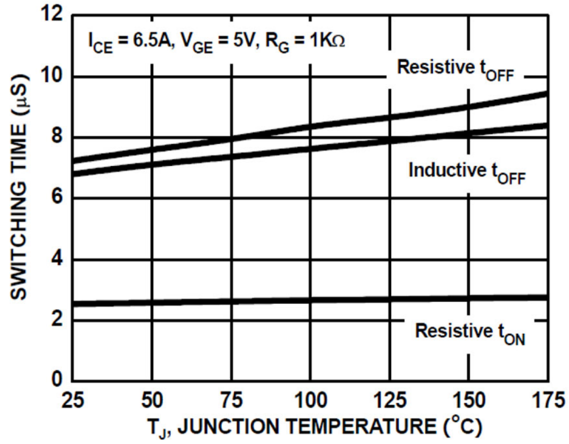


Figure 13. Switching Time vs. Junction Temperature

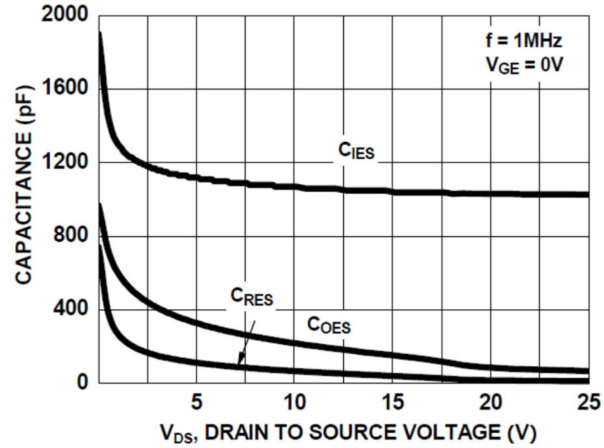


Figure 14. Capacitance vs. Collector to Emitter

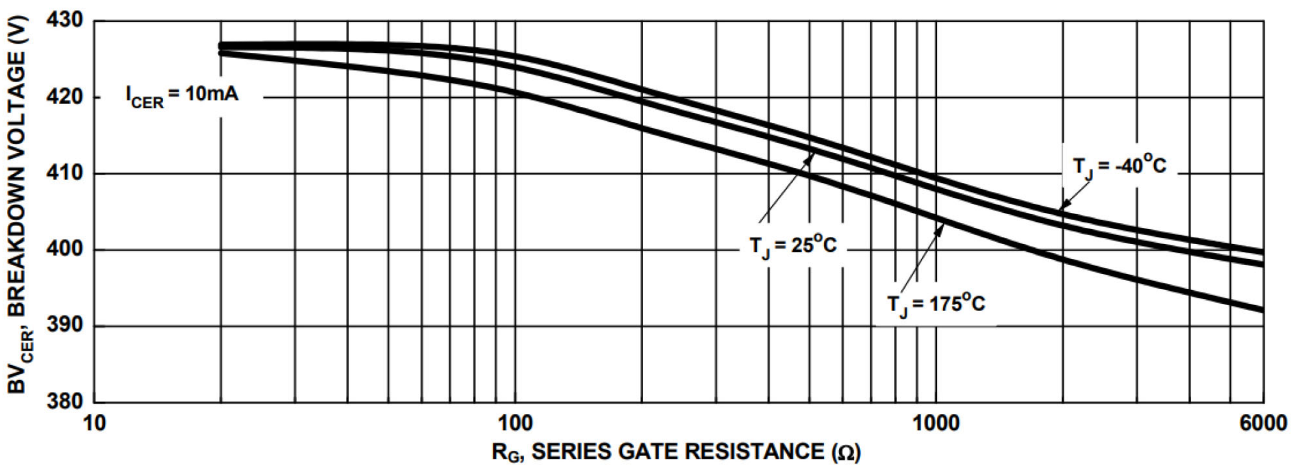


Figure 15. Break Down Voltage vs. Series Resistance

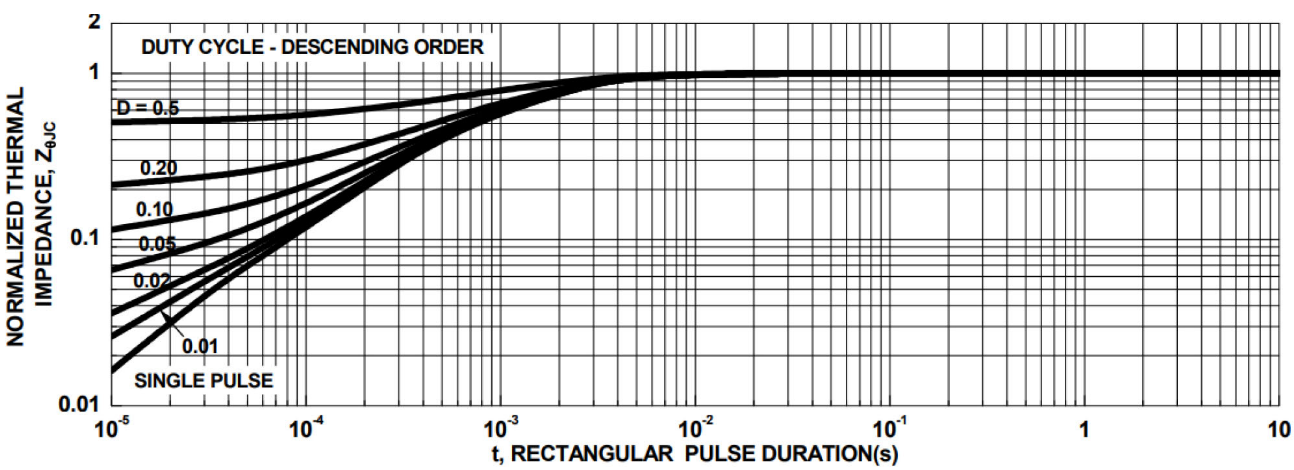


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TEST CIRCUIT AND WAVEFORMS

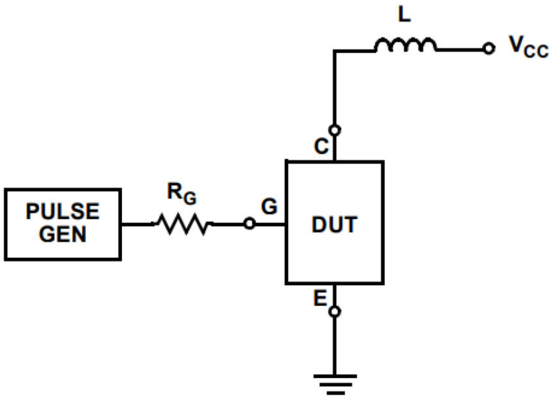


Figure 17. Inductive Switching Test Circuit

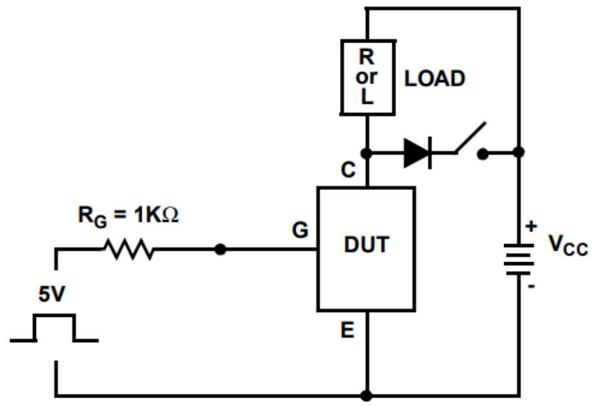


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

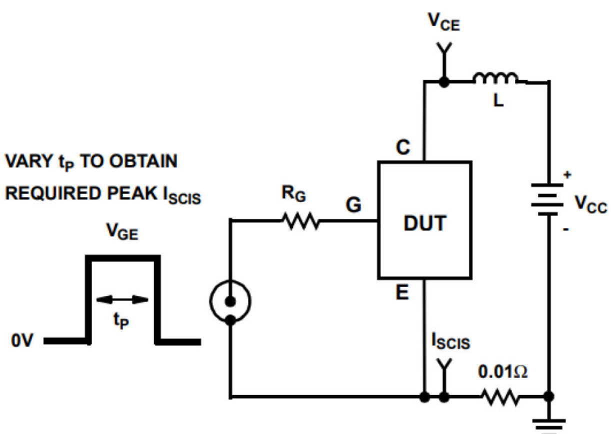


Figure 19. Energy Test Circuit

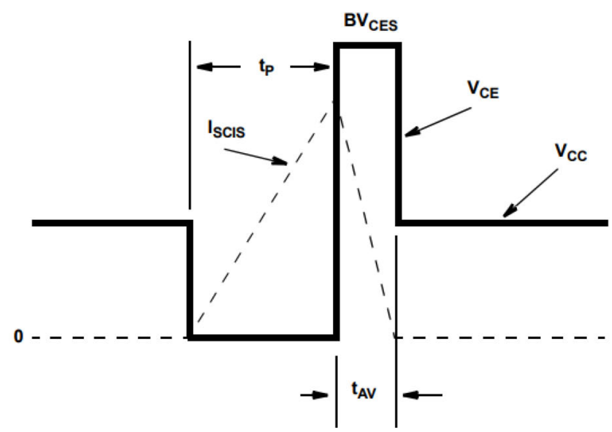


Figure 20. Energy Waveforms

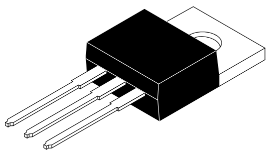
PACKAGE MARKING AND ORDERING INFORMATION

Device	Package	Shipping†
ISL9V3040D3ST−F085C	DPAK (Pb−Free)	2500 Units/Tape & Reel
ISL9V3040S3ST−F085C	D2PAK (Pb−Free)	800 Units/Tape & Reel
ISL9V3040P3−F085C	TO220 (Pb−Free)	50 Units/Tube

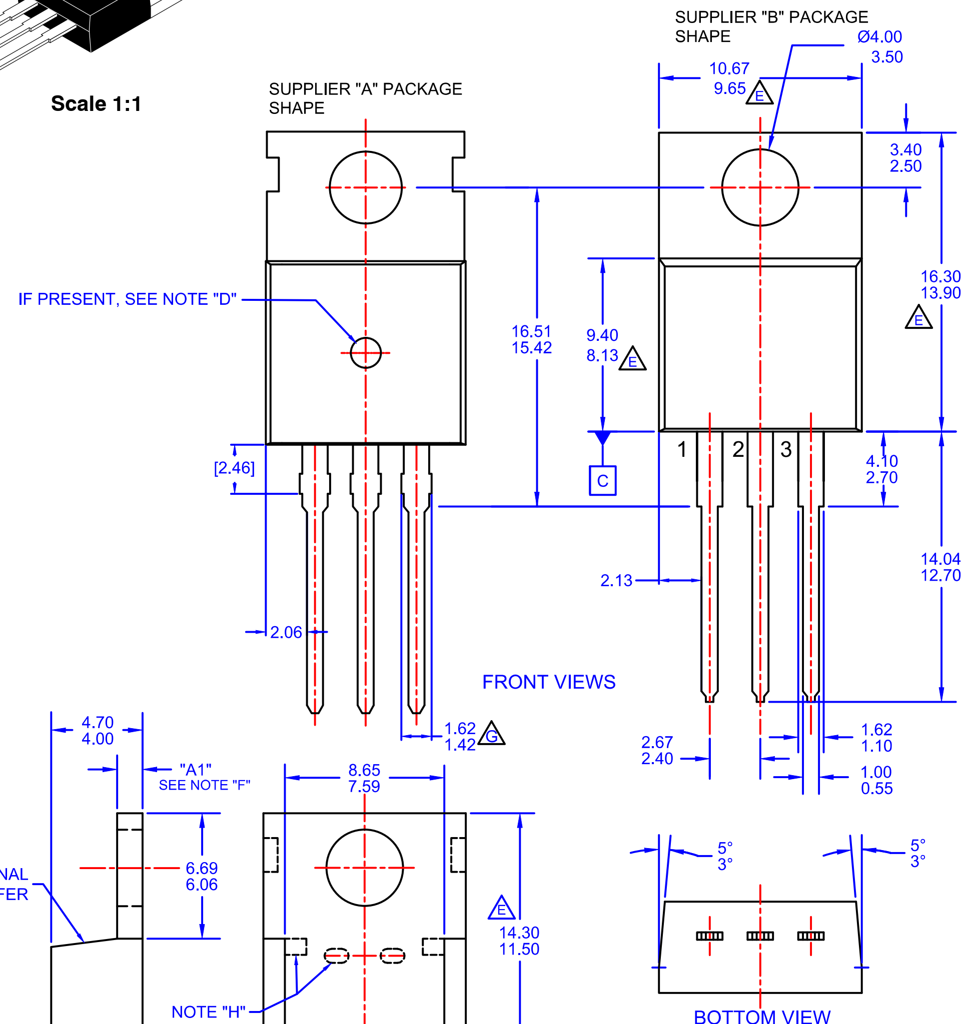
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

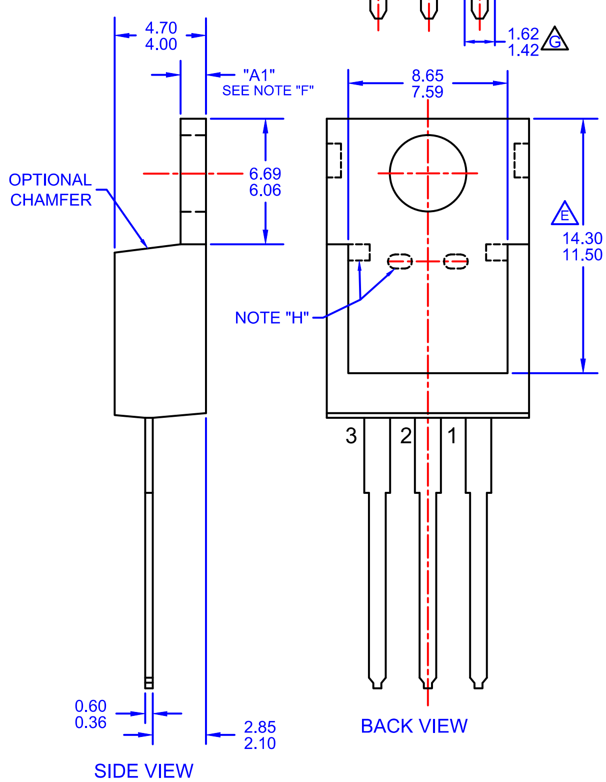
TO–220–3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1





NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G) PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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DESCRIPTION:	**TO–220–3LD**	**PAGE 1 OF 1**

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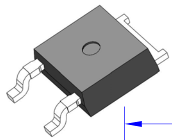
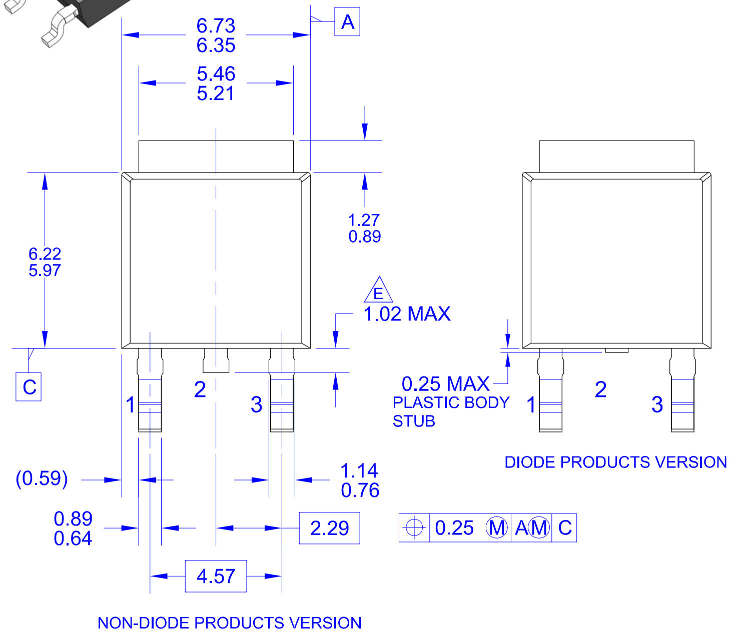
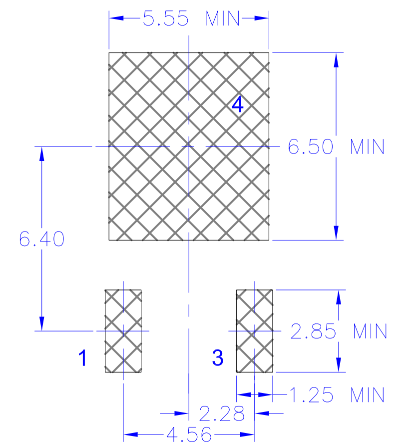


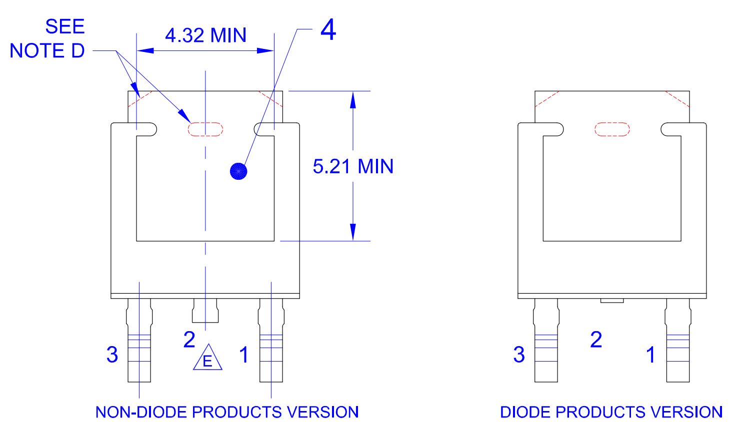
DPAK3 (TO−252 3 LD)
CASE 369AS
ISSUE O

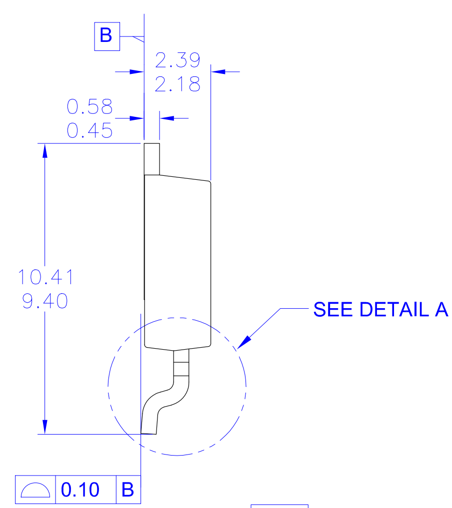
DATE 30 SEP 2016



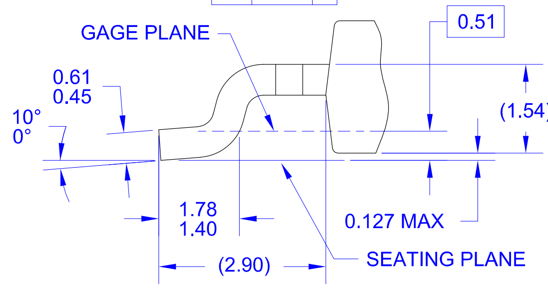


LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

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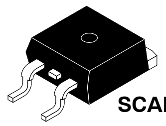
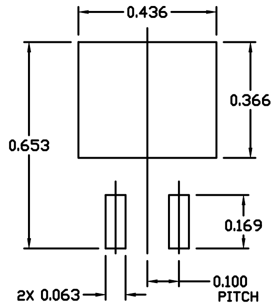


SCALE 1:1

D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021

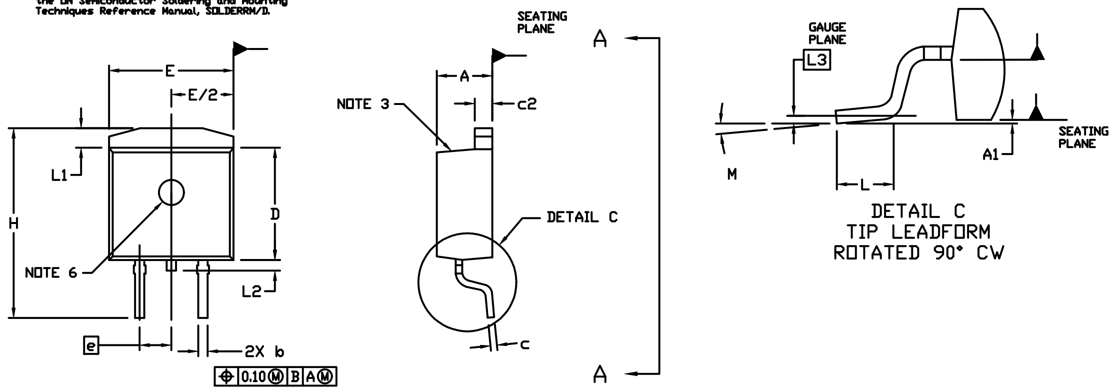


RECOMMENDED MOUNTING FOOTPRINT

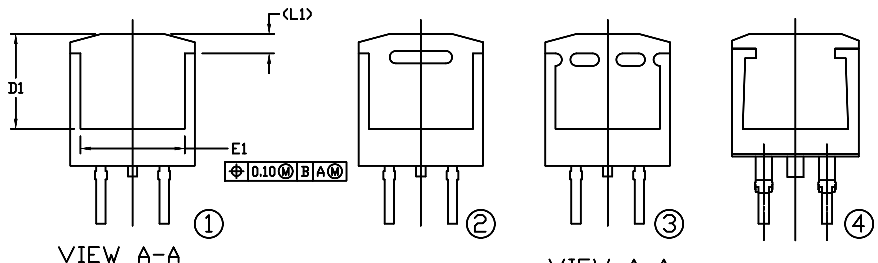
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°



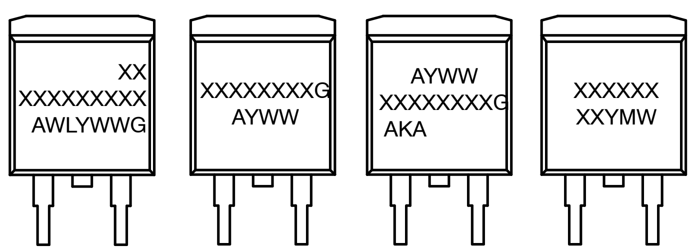
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A-A

VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC   Standard   Rectifier   SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON56370E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	D²PAK−3 (TO−263, 3−LEAD)	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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