NCP5371

High Efficiency Synchronous Rectifying IMVP6 Notebook Controller

This controller is specifically designed to support the INTEL notebook RS – IMVP6 Mobile Processor power delivery requirements. The current mode variable frequency architecture provides ultra fast dynamic response with virtually no overshoot for dynamic loads and dynamic VID changes. The feed−forward on time control virtually eliminates the effects of input voltage variations. The gate drivers are optimized to drive large Qg low−side trench devices for maximum overall system efficiency.

Features

- Automatic Variable Frequency Operation for Light Load Power Savings
- Supports 2 Phase Control
- Differential Voltage Sensing
- Differential Lossless Inductor Current Sensing
- Undervoltage Lockout
- Overvoltage Protection
- Thermal Shutdown Protection
- Ultra Low Current Consumption when Disabled
- This is a Pb−Free Device

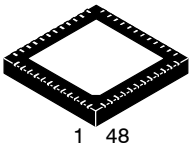
Application

- Notebooks

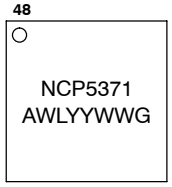
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



QFN48
MN SUFFIX
CASE 485K



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NCP5371MNR2G	QFN (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

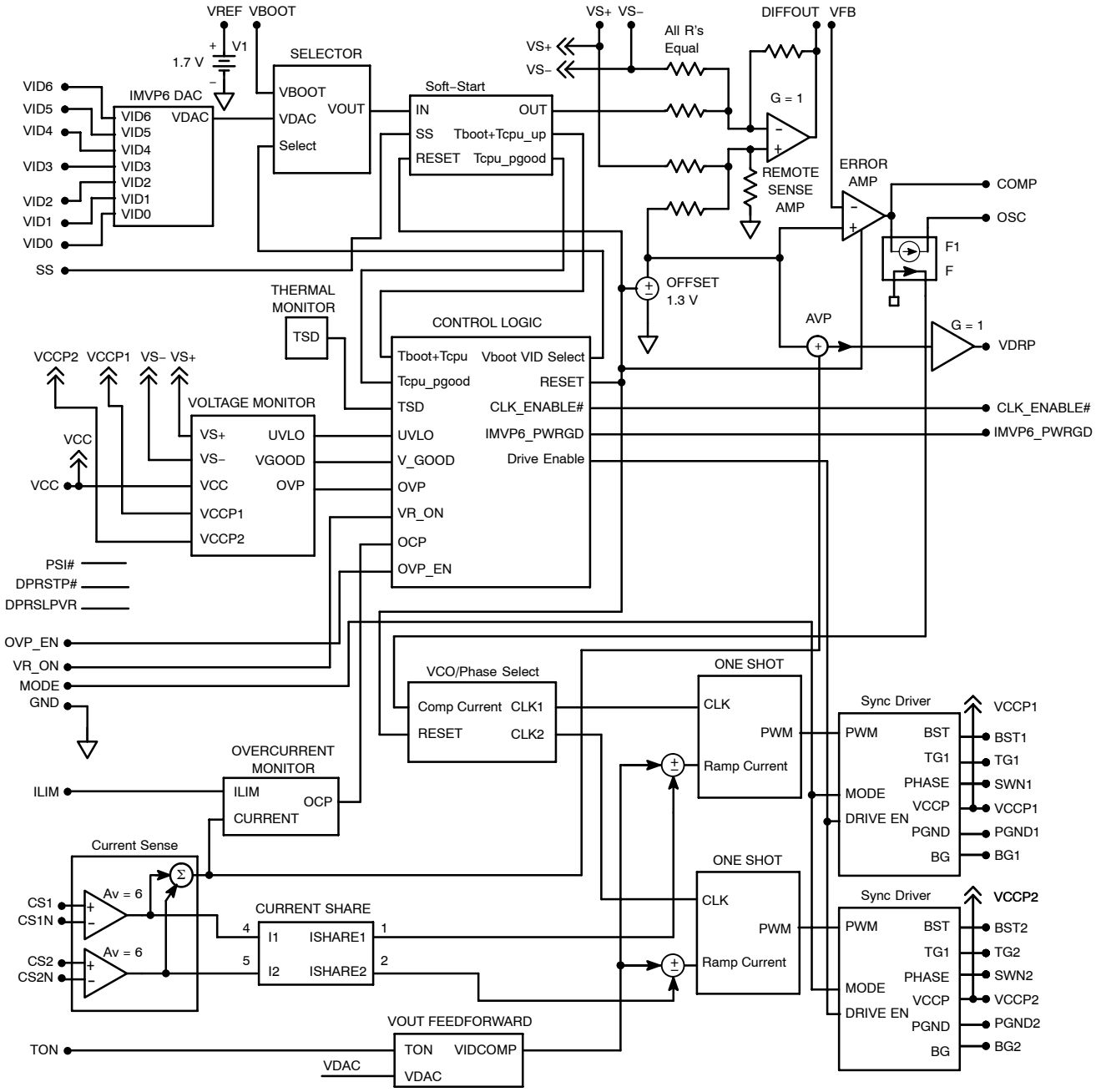


Figure 1. Block Diagram

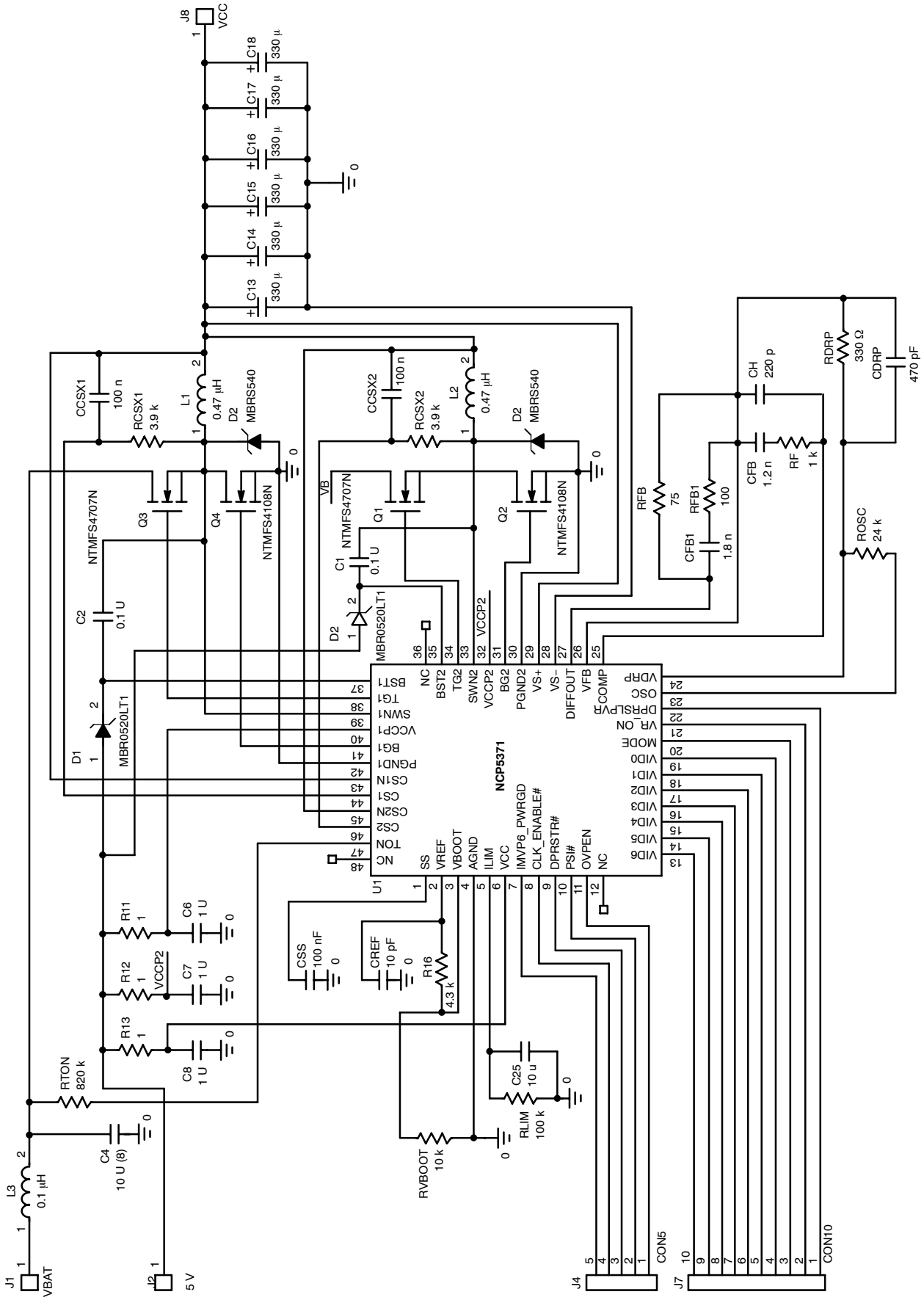


Figure 2. Two Phase Application Circuit

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	SS	Soft−start control pin with 40 μA (type) current pulling out.
2	VREF	1.7 V reference for VBOOT.
3	VBOOT	Boot Voltage Input.
4	AGND	Analog ground connection and remote ground sense.
5	ILIM	Current limit adjustment pin (pull to V_{CC} to disable ILIM).
6	VCC	Power for the analog and control sections of the IC.
7	IMVP6_PWRGD	IMVP6 Power good signal open−drain output.
8	CLK_ENABLE#	IMVP6 Clock Enable signal open−drain output.
9	DPRSTP#	IMVP Power Saving Logic Input (See Table 2).
10	PSI#	IMVP Power Saving Logic Input (See Table 2).
11	OVP_EN	Enables Overvoltage Protection.
12	NC	−
13	VID6	DAC BIT
14	VID5	DAC BIT
15	VID4	DAC BIT
16	VID3	DAC BIT
17	VID2	DAC BIT
18	VID1	DAC BIT
19	VID0	DAC BIT
20	MODE	Logic High Input enables negative current limit. Logic Low to allow PSI# and PRRSTR# to control.
21	VR_ON	Logic Input that enables, disables, and resets the controller.
22	DPRSLPVR	Deeper Sleep Mode signal for slow slew rate setting.
23	OSC	Voltage control oscillator (VCO) gain control pin.
24	VDRP	Total inductor current signal output for droop compensation.
25	COMP	Error amplifier output for feedback compensation.
26	VFB	Error amplifier inverting input for feedback compensation.
27	DIFFOUT	Output voltage error.
28	VS−	Output voltage remote ground sense.
29	VS+	Output voltage remote sense.
30	PGND2	Ground return for the high current.
31	BG2	Phase 2 bottom gate drive.
32	VCCP2	Power for the high current driver section of the IC.
33	SWN2	Phase 2 top gate floating switch node return.
34	TG2	Phase 2 top gate drive.
35	BST2	Phase 2 top gate driver power input.
36	NC	−
37	BST1	Phase 1 top gate driver power input.
38	TG1	Phase 1 top gate drive.
39	SWN1	Phase 1 top gate floating switch node return.
40	VCCP1	Power for the high current driver section of the IC.
41	BG1	Phase 1 bottom gate drive.
42	PGND1	Ground return for the high current.
43	CS1N	Negative differential current sense pin for phase 1.
44	CS1	Positive differential current sense pin for phase 1.
45	CS2N	Negative differential current sense pin for phase 2.
46	CS2	Positive differential current sense pin for phase 2.
47	TON	On time control pin (Provides Feed Forward and Frequency Control).
48	NC	−

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} (Pin 6) to PGND	V_{CC}	−0.3, 7.0	V
V_{CCP1}, V_{CCP2} (Pin 33, 39) to PGND	V_{CCP}	−0.3, 7.0	V
TON (Pin 47) to PGND	V_{TON}	−0.3, 30	V
BST1, BST2 (Pin 35,37) wrt SWN1, SWN2	V_{BST}−$V_{SWN(*)}$	−0.3, 7.0	V
SWN1, SWN2 (Pin 33, 39) to PGND	V_{SWN}	−5.0 (<100 ns) −0.3 (DC), 30	V
VS+, VS− (Pin 28−29) to PGND	V_S	−0.3, 7.0	V
CS1, CS1N, CS2, CS2N (Pin 43−46) to PGND	V_{CS}	−0.3, 7.0	V
VID0−VID6, MODE, VR_ON (Pin 13−19, 20, 21) to PGND	V_{vid}	−0.3, 7.0	V
SS, IMVP6_PWRGD, CLK_ENABLE#, DPRSTP#, PSI#, OVP_EN, OSC, VDRP, VFB, COMP, DIFFOUT (Pin 1, 7−11, 22−23, 25−27) to PGND	V_{IO}	−0.3, 7.0	V
Gate Drive TG1, TG2 (Pin 34, 38) wrt SWN1, SWN2	V_{TG}− V_{SWN}	−0.3, 7.0	V
Gate Drive BG1, BG2 (Pin 31, 41) to PGND	V_{BG}	−2.0 (<100 ns), −0.3 (DC), 7.0	V
PGND1, PGND2 (Pin 30, 42) to AGND (Pin 4)	V_{GND}	−0.3, 0.3	V
V_{REF} (Pin 2) to PGND	V_{REF}	−0.3, 7.0	V
V_{BOOT} (Pin 3) to PGND	V_{BOOT}	−0.3, 7.0	V
I_{LIM} (Pin 4) to PGND	V_{ILIM}	−0.3, 7.0	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Based on 30 V MOSFET maximum rating.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
QFN Exp Pad Thermal Resistance Junction−to−Ambient	$R_{\theta JA}$	35	°C/W
QFN Exp Pad Thermal Resistance Junction−to−Case	$R_{\theta JC}$	TBD	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature Soldering, Reflow (SMD Styles Only)	−	260 Peak	°C
Moisture Sensitivity Level	MSL	1	−

2. This device series incorporates ESD protection and exceeds the following ratings:
   Human Body Model (HBM) ≤2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ≤200 V per JEDEC standard: JESD22−A115.
3. Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78.

ELECTRICAL CHARACTERISTICS (Circuit of Figure 2, V_{CC} = V_{CCP1} = V_{CCP2} = 5.0 V, V (V_{s+}, V_{S-}) = VID (0011000) = 1.2 V, T_A = −40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
CONTROLLER						
Input Voltage Range	V_{BAT}	Battery Voltage (Feedforward voltage from V_{BAT} to T_{ON} connected by a 1 Meg ohm resistor)	7.0	12	28	V
	V_{CC}, V_{CCP1}, V_{CCP2}	–	4.5	5.0	5.5	–
DC Output Voltage Accuracy	V (VS +, VS–)	VID codes for 1.5 V to 0.7625 V, 44 A Maximum Load	–	–	±1.5	%
		VID codes for 0.75 V to 0.5 V, 44 A Maximum Load	–	–	±11.5	mV
		VID codes for 0.4875 V to 0.3 V, 3.0 A Maximum Load	–	–	±25	mV
VCC POWER SUPPLY						
Supply Current, Normal Operating	I_{VCC}	FS = 400 k	–	10	20	mA
Supply Current, Shutdown	I_{VCC_SD}	–	–	10	40	μA
VCCP1 POWER SUPPLY						
Supply Current, Normal Operating	I_{VCCP1}	FS = 400 k (3.3 nF capacitor in BG)	–	10	–	mA
Supply Current, Shutdown	I_{VCCP1_SD}	–	–	10	20	μA
VCCP2 POWER SUPPLY						
Supply Current, Normal Operating	I_{VCCP2}	FS = 400 k (3.3 nF capacitor in BG)	–	10	–	mA
Supply Current, Shutdown	I_{VCCP2_SD}	–	–	10	20	μA
BST1 POWER SUPPLY						
Supply Current, Shutdown	I_{BST1_SD}	–	–	10	20	μA
BST2 POWER SUPPLY						
Supply Current, Shutdown	I_{BST2_SD}	–	–	10	20	μA
THERMAL SHUTDOWN						
Overtemperature Trip Point	TSD	–	–	150	–	°C
Hysteresis	TSD_{hys}	–	–	30	–	°C
UNDERVOLTAGE LOCKOUT						
V_{CC} Start Threshold	VCC_{th}	–	4.05	4.25	4.48	V
Hysteresis	VCC_{hys}	–	–	275	–	mV
V_{CCP} Start Threshold	$VCCP_{th}$	–	4.05	4.25	4.48	V
Hysteresis	$VCCP_{hys}$	–	–	275	–	mV
FAULT PROTECTION AND POWER OFF						
Output Overvoltage Protection Threshold	VOVP	OVPEN = V_{CC}	–	1.625	1.7	V
Delay between VR_ON Deassertion and PWRGD Deassertion	$T_{PWRDOWN1}$	–	–	–	100	ns
Delay between PWRGD Deassertion and VR Output Rail Ramping Down	$T_{PWRDOWN2}$	(Note 4)	–	–	100	ns

4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) (Circuit of Figure 2, V_{CC} = V_{CCP1} = V_{CCP2} = 5.0 V, V (V_{s+}, V_{S-}) = VID (0011000) = 1.2 V, T_A = −40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
VR_ON INPUT CHARACTERISTICS						
Logic High Threshold	$VRON_H$	–	0.6	–	–	V
Logic Low Threshold	$VRON_L$	–	–	–	0.4	V
VR_ON Leakage Current	IRONL	–	−1.0	–	1.0	μA
NEGATIVE CURRENT LIMITER						
Trip Threshold (SWN to GND)	NC_{th}	–	–	−1.0	–	mV
Blanking Delay	NC_{BDly}	–	–	100	–	ns
HIGH SIDE DRIVE						
Non−Overlap Time, UG Going High	$tpdh_{UG}$	BG 90% to TG 10%	–	40	–	ns
Output Resistance (Sourcing)	RHS_{source}	Force 5.0 – 0.4 V to TG	–	1.0	4.0	Ω
Output Resistance (Sinking)	RHS_{sink}	Force 0.4 V to TG	–	1.0	4.0	Ω
Upper Gate Drive Pulldown Resistor	RHS_{PD}	Force 0.4 V to TG	–	60	–	kΩ
LOW SIDE DRIVE						
Non−Overlap Time, LG Going High	$tpdh_{LG}$	TG 90% to BG 10%	–	40	–	ns
Output Resistance (Sourcing)	RLS_{source}	Force 5.0 – 0.4 V to TG	–	1.0	4.0	Ω
Output Resistance (Sinking)	RLS_{sink}	Force 0.4 V to TG	–	0.4	2.0	Ω
Gate Drive Pulldown Resistor	RLS_{PD}	Force 0.4 V to TG	–	60	–	kΩ
ERROR AMPLIFIER						
Input Offset Voltage	VOS_{EA}	(Note 5)	−1.5	–	1.5	mV
Output Voltage Swing	$VOSwing_{EA}$		1.0	–	3.0	V
Gain−Bandwidth Product	GBW_{EA}	Load = 100 pF GND	–	15	–	MHz
Phase Margin	PM_{EA}	Unity Gain with 100 pF Load	–	40	–	deg
Gain	$Gain_{EA}$	RL = 10 k to GND, Inputs at 1.0 V	–	81	–	dB
Slew Rate	SR_{EA}	Capacitive Load of 100 pF, ±100 mV Steps	–	±2.0	–	V/μs
Source Current	$ISource_{EA}$	COMP = 3.0 V	2.0	4.0	–	mA
Sink Current	$ISink_{EA}$	COMP = 3.0 V	2.0	4.0	–	mA
REMOTE SENSE AMPLIFIER						
Input Offset Voltage	VOS_{RSA}	(Note 5)	−1.5	–	1.5	mV
V (VS+, VS−) to DIFFOUT Gain	$Gain_{RSA}$	–	0.99	1.0	1.01	V/V
Max Output Voltage Swing	$VOS_{maxwingRSA}$	VS+ = 3 V, Max RSA Voltage	3.0	–	–	V
Min Output Voltage Swing	$VOS_{minwingRSA}$	VS+ = 0.1 V, Min RSA Voltage	–	–	0.4	V
VS+ and VS− Input Signal Range	VIN_{RSA}	–	0	–	3.0	V
3.0 dB Bandwidth	BW_{RSA}	–	–	20	–	MHz
Source Current	$Isource_{RSA}$	–	3.0	5.0	–	mA
Sink Current	$Isink_{RSA}$	–	1.0	1.5	–	mA

5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) (Circuit of Figure 2, V_{CC} = V_{CCP1} = V_{CCP2} = 5.0 V, V (V_{s+}, V_{S-}) = VID (0011000) = 1.2 V, T_A = −40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Minimum Operating Frequency	$Fosc_{min}$	–	–	0	–	–
Maximum Operating Frequency	$Fosc_{max}$	(each phase) R_{OSC} = 30 kΩ, V_{COMP} − V_{OSC} = 3.0 V	–	3.0	–	MHz
OSC Current to Frequency Gain	VCO_{Gain}	–	–	25	–	MHz/ mA
VDROOP AMPLIFIER						
Max Output Voltage Swing	VOS_{MaxDrp}	(Note 6)	3.0	–	–	V
Min Output Voltage Swing	VOS_{MinDrp}	(Note 6)	–	–	1.0	V
Gain−Bandwidth Product	GBW_{Drp}	Load = 100 pF to GND	–	15	–	MHz
Phase Margin	PM_{Drp}	Unity Gain	–	40	–	deg
Gain	$Gain_{Drp}$	RL = 10 k to GND	–	81	–	dB
Slew Rate	SR_{Drp}	Capacitive Load of 100 pF, ±100 mV Steps	–	±2.0	–	V/μs
Source Current	$ISource_{Drp}$	V_{DROOP} = 3.0V, 0.2V of Overdrive	1.0	4.0	–	mA
Sink Current	$ISink_{Drp}$	V_{DROOP} = 1.2V, 0.2V of Overdrive	1.0	4.0	–	mA
CS1 to Voltage of DRPGain	$V_{cs1drpg}$	–	–	6.0	–	V/V
CS2 to Voltage of DRPGain	$V_{cs2drpg}$	–	–	6.0	–	V/V
ONE SHOT						
Minimum On Time Allowed	TON_{min}	(Note 6)	–	–	100	ns
Phase to Phase On Time Matching	Ph_{match}	CSx−CSNx = 0	−10	–	10	%
TON						
On Time for each Phase	TON	RTON = 2.0 M, VBAT = 12, CSx − CSNx = 0	–	850	–	ns
		RTON = 1.0 M, VBAT = 12, CSx − CSNx = 0	400	500	600	ns
		RTON = 500 k, VBAT = 12, CSx − CSNx = 0	–	290	–	ns
Input Bias Current when Disabled	$ITON_{SD}$	VTON = 18 V	–	–	10	μA
VREF						
Output Voltage	VREF	–	–	1.7	–	V
Tolerance	$VREF_{tol}$	No Load	–	–	±1.0	%
Source Current	$IREF_{out}$	–	100	–	–	μA
CURRENT LIMIT						
ILIM Bias Current	$ILIM_{bias}$	–	9.0	10	11	μA
ILIM Threshold Accuracy, V (CS1, CS1N) + V (CS2, CS2N)−VLIM	Vth_{ILIM}	V (CSx, CSxN) = 25 mV, Vth_{ILIM} = V_{LIM} − 25 mV*6	–	0	–	mV
Current Limit Range	$Range_{ILIM}$	(Note 6)	0.3	–	2.0	V

6. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued) (Circuit of Figure 2, V_{CC} = V_{CCP1} = V_{CCP2} = 5.0 V, V (V_{s+}, V_{S-}) = VID (0011000) = 1.2 V, T_A = −40 to 85°C, unless other noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
IMVP6_PWRGD						
Delay from CLK_ENABLE#	$TDlyCK_{PWRGD}$	–	3.0	–	10	mS
Logic Low	$PWRGD_L$	500 Ω Pullup to 3.3 V	–	–	0.3	V
OFF State Leakage Current	$IOFFL_{PWRGD}$	–	–	–	100	μA
Power Good Tolerance Positive Side	PWRGDTP	–	–	200	–	mV
Power Good Tolerance Negative Side	PWRGDTN	–	–	−300	–	mV
Power Not Good Indicate Banding Windows	TPWRNGD	–	–	200	–	μS
CLK_ENABLE#						
Delay from Vboot	Tboot+Tcpu_up	–	20	–	130	μS
Logic Low	$CKENB_L$	500 Ω Pullup to 3.3 V (Note 7)	–	–	0.3	V
OFF State Leakage Current	$IOFFL_{CKENB}$	–	–	–	10	μA
SOFT−START						
SS Soft−Start Current	I_{SS}	–	32	40	48	μA
VID INPUTS						
De Bounce/De Skew Time	$TDeSkew_{VID}$	(Note 7)	100	–	–	nS
Logic High Threshold	VH_{VID}	–	650	–	–	mV
Logic Low Threshold	VL_{VID}	–	–	–	350	mV
Input Leakage Current	$ILEA_{VID}$	VID0, VID1, VID2, VID3, VID4, VID5, VID6	–	–	10	μA
VDAC OUTPUT						
Slew Rate	SRvs	DPRSTP#0, DPRSLPVR 1 or DPRSTP#1, DPRSLPVR 0	8.75	–	–	mV/μs
Slow Slew Rate	SSRvs	DPRSTP#1, DPRSLPVR 1	1.75	–	–	mV/μs
DPRSLPVR# AND DPRSTP# INPUTS						
Logic High Threshold	VH_{Logic}	–	650	–	–	mV
Logic Low Threshold	VL_{Logic}	–	–	–	350	mV
Input Leakage Current	$ILEA_{Logic}$	DPRSLPVR#, DPRSTR#	–	–	30	μA
PSI#, MODE, INPUTS						
Logic High Threshold	VH_{Logic}	–	650	–	–	mV
Logic Low Threshold	VL_{Logic}	–	–	–	350	mV
Input Leakage Current	$ILEA_{Logic}$	PSI#, MODE	–	–	10	μA
OVP_EN INPUTS						
Logic High Threshold	VH_{Logic}	–	650	–	–	mV
Logic Low Threshold	VL_{Logic}	–	–	–	350	mV

7. Guaranteed by design.

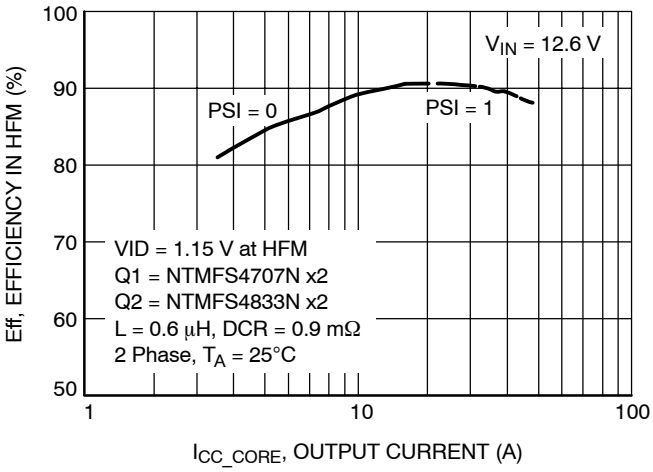


Figure 3. Efficiency in HFM vs. Output Current

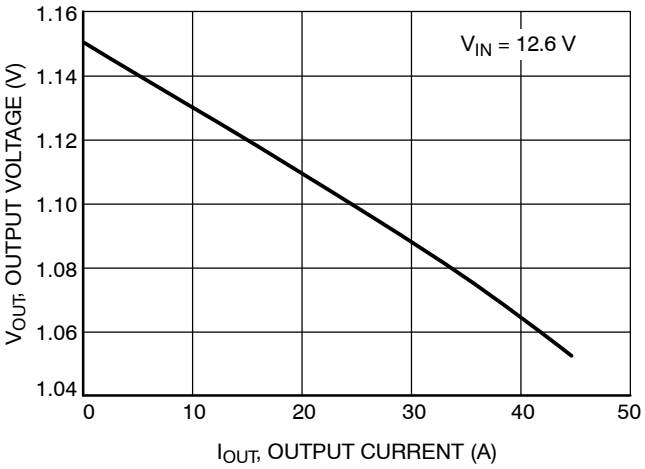


Figure 4. Output Voltage vs. Output Current

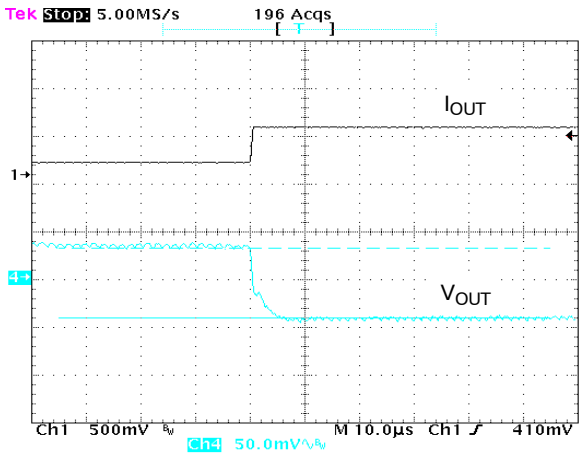


Figure 5. Load step−up response via LGA775 Ver 2 VTT 9A−44A load step @200 A/μs

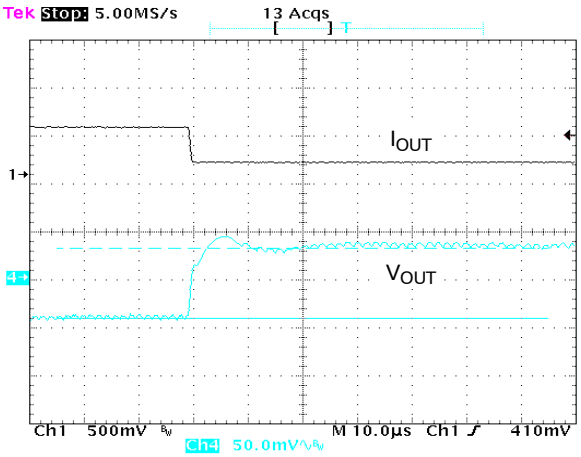


Figure 6. Load dump responses via LGA775 Ver 2 VTT 44A−9A load step @200 A/μs

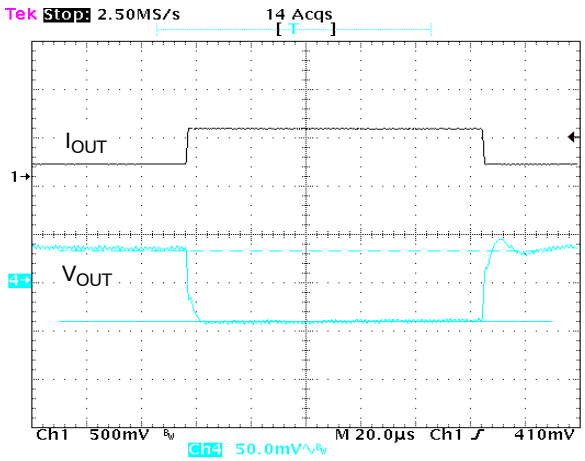


Figure 7. Load responses via LGA775 Ver 2 VTT 9A−44A−9A load step @200 A/μs

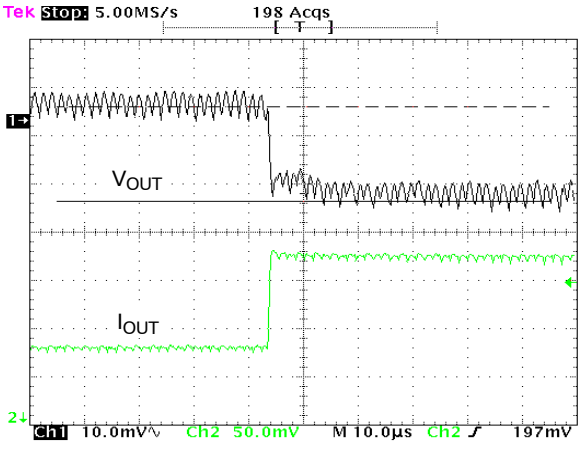


Figure 8. Load step via LGA775 Ver 2 VTT 9A−18A load step @200 A/μs

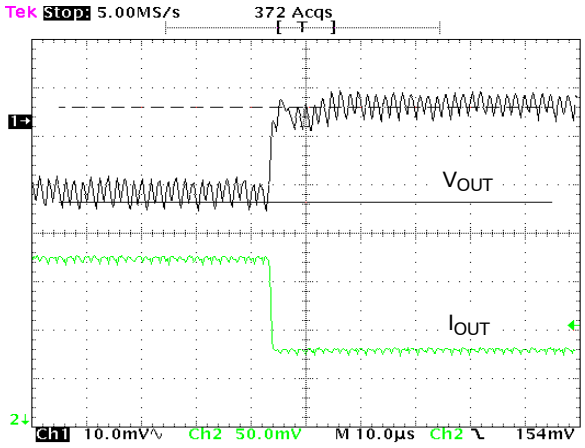


Figure 9. Load dump responses via LGA775 Ver 2 VTT 18A−9A load step @200 A/µs

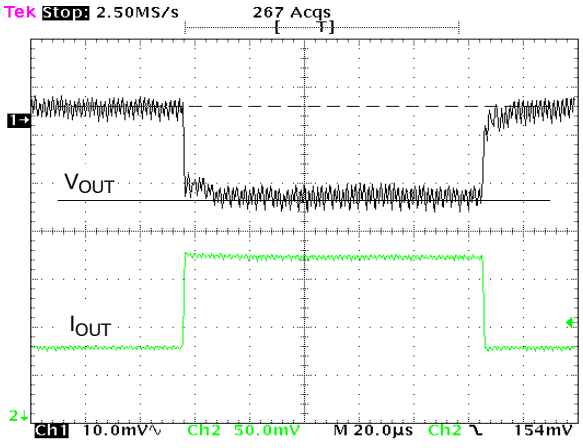


Figure 10. Load responses via LGA775 Ver 2 VTT 9A−18A−9A load step @200 A/µs

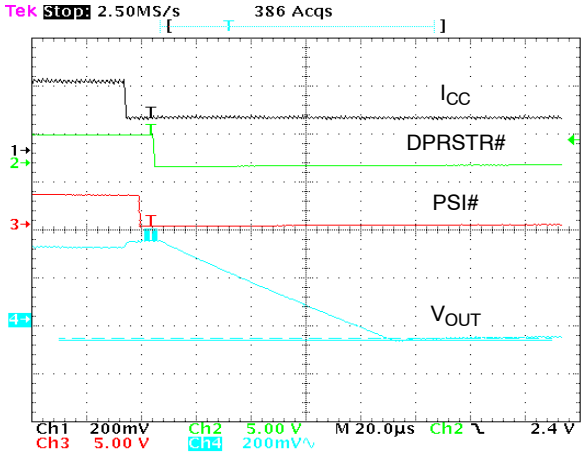


Figure 11. C4 Entry with LGA775 Ver 2 VTT

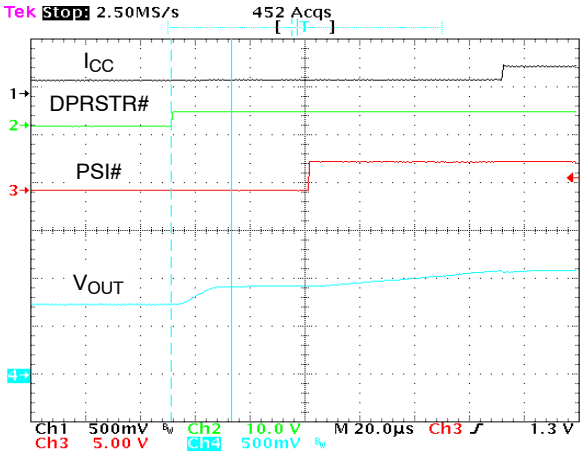


Figure 12. C4 Exit with LGA775 Ver 2 VTT

OPERATING DESCRIPTION

General

The NCP5371 is a 2 phase PWM controller specifically designed to address the requirements of Intel IMVP6 specification. The variable frequency architecture is designed to provide high efficiency under light load conditions, excellent input rejection, fast dynamic VID response, and rapid recovery from transient load conditions.

Soft−Start

During soft−start, the output voltage must ramp up linearly in a slowly controlled manner. The Vboot voltage for IMVP6 is expected to be 1.2 V but may be as high as 1.53 or as low as 1.0 V. The SS pin will be loaded with a 0.1 μF capacitor. The capacitor would be ensured discharge before charging. A 40 μA bias current is applied to the SS pin to create the soft−start ramp signal. The DAC voltage will be limited by the rising soft−start voltage which creates a ramped reference for the controller to follow up in a controlled manner.

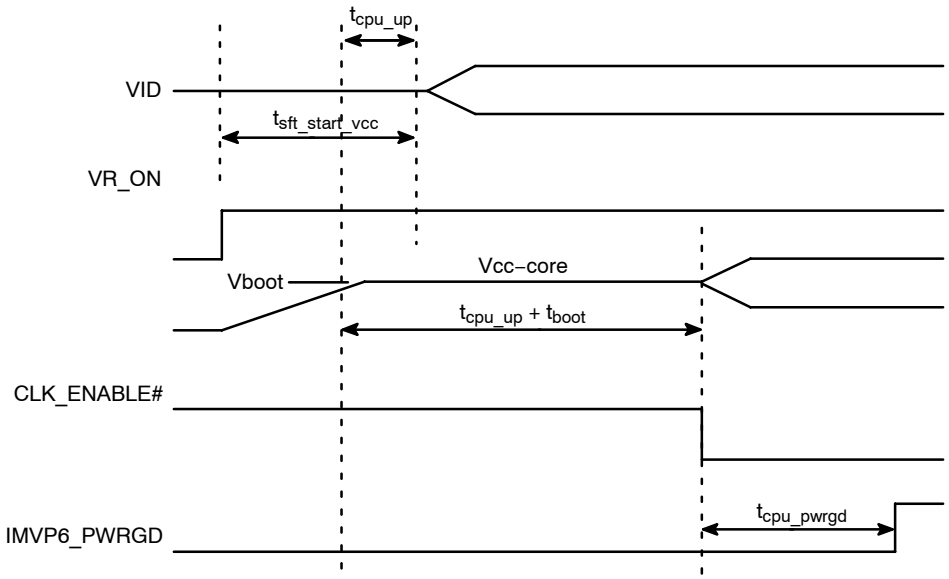


Figure 13. Startup Timing Diagram

VID Inputs

Once the output almost achieves Vboot, a 75 μS timer will be initialized and the VID code will be captured. After the timer expires, the new DAC voltage will be applied to the controller to follow but the change will NOT be limited by the soft−start ramp any more.

However, when the reference is switched from 0 V to a DAC voltage, the soft−start ramp control will be applied in order to limit the transient input current consumption from VBAT.

VID SELECTOR

The VID at startup will be externally programmed by a resistor divider from Vref. When Vcore almost reaches Vboot, the external VID code is selected and applied to controller after the timing of Tcpu + Tboot. See Soft−start Timing shown in Figure 13.

OUTPUT TOLERANCE ANALYSIS

The DAC Tolerance minimum requirement was back calculated from the overall system regulation requirements. **The DAC regulation requirement is measured across VS+ and VS− pins.**

Requirements

2.1 mΩ Load Line

1.5 V–0.7625 V	± 1.5% Total System Tolerance (Excludes Ripple)	44 A Maximum Load
0.75 V–0.5 V	± 11.5 mV Total System Tolerance (Excludes Ripple)	44 A Maximum Load
0.4875–0.3 V	± 25 mV Total System Tolerance (Excludes Ripple)	3.0 A Maximum Load

Note: CODE 1111111 is a special off code condition where the controller is disabled but indicating power good.

Table 1. VID (Only monotonicity can be guaranteed to decrement when Vout is lower than 0.25 V)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000

Table 1. VID (continued) (Only monotonicity can be guaranteed to decrement when Vout is lower than 0.25 V)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000

Table 1. VID (continued) (Only monotonicity can be guaranteed to decrement when Vout is lower than 0.25 V)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000

Table 1. VID (continued) (Only monotonicity can be guaranteed to decrement when Vout is lower than 0.25 V)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

DAC Slew Rate

The DAC output is slew rate limited to prevent overshoot of the system output voltage. If the DAC voltage rises significantly faster than that the control system can be achieved, the output voltage will overshoot. The DAC slew rate is limited between 10 mV/μS and 15 mV/μs.

Voltage Controlled Oscillator

The VCO is critical to the transient response of the overall system. When the load is stepped, the clock will turn on the next phase's one shot as fast as possible.

Current Sharing Function

By default, the one shot on times for both phases will be determined by the external resistor connected to TON, which is used to ramp up the coil currents. Because of various reasons, the coil currents would not be match.

If V (CS1,CS1N) is larger than V (CS2,CS2N), the on time for Phase 1 and Phase 2 will be reduced and increased respectively. The amount of adjustment will be based on their difference proportionally. (The detail amount of the adjustment will be provided later.) The same operation would be applied when V (CS2,CS2N) is greater than V (CS1,CS1N).

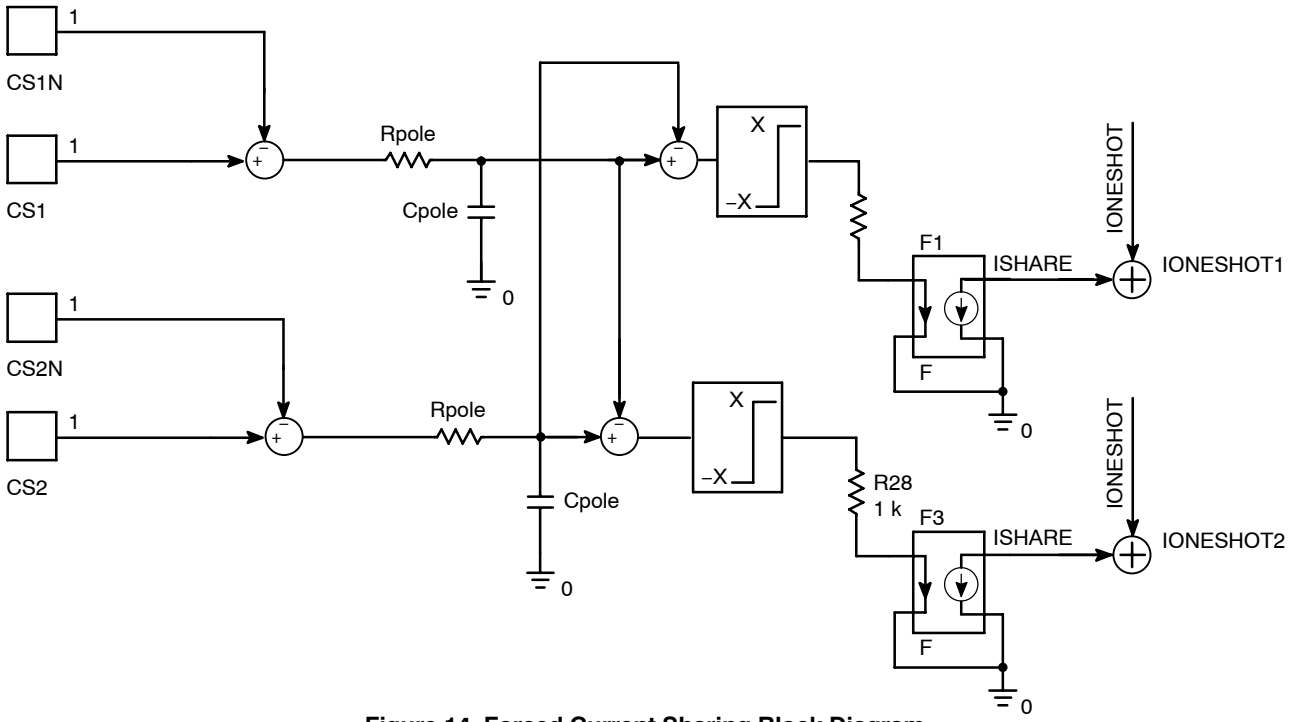


Figure 14. Forced Current Sharing Block Diagram

Forced−PWM Mode (DPRSTP# = HIGH, PSI# = LOW or DPRSTP# = LOW, PSI# = HIGH)

The forced−PWM mode disables the zero−crossing comparator, allowing the inductor current to reverse at light loads. This causes the low−side gate−drive waveform to become the complement of the high−side gate−drive waveform. Forced PWM mode is required during downward output voltage transitions. The following table shows the logic combination of pin DPRSTP# and PSI#.

Table 2. Forced−PWM Mode

MODE	DPRSTR#	PSI#	
1	X	X	Negative Current Detection ON, Allow DCM Operation at Light Load
0	0	0	Negative Current Detection ON, Allow DCM Operation at Light Load
0	0	1	Forced PWM Mode, Only CCM Operation
0	1	0	Forced PWM Mode, Only CCM Operation
0	1	1	Negative Current Detection ON, Allow DCM Operation at Light Load

Current Sensing

The current sense amplifiers must provide enough bandwidth and slew rate to generate an accurate representation of the sensed current waveform at the maximum operating frequency. The current sensing has very low offset voltage so as to provide accurate droop control and current sharing. The sensed current voltage is gained by six and summed with the offset reference voltage from the droop amplifier. The individual current sense signals are reused in the current sharing function. The current sense signals for each phase is typically max. 100 mV.

Current Sense to Droop Transfer Function and Amplifiers

The droop signal should be an accurate representation of the summed current sense waveforms and the amplifiers must be stable over a wide range of external loads.

VR_ON

It is the enable for the controller. When the controller is disabled by VR_ON the internal state machines must be reset into a known starting state to prepare for soft−start. For the fault conditions of overvoltage or overcurrent, it is used to restart the power cycle.

Feed−Forward

The controller provides both VIN and VID feed−forward. For the VIN feed−forward, TON depends on VIN change. When VIN increases, TON decreases accordingly to fix the time of period. Similarly, for the VID feed−forward, TON also depends on VID change. When VID increases, TON increases accordingly to fix the time of period. They give the equation.

$$Tperiod = VIN/VOUT * TON \qquad \text{(eq. 1)}$$

TON Selection

With minimum VOUT and maximum VIN, the TON must be NOT LESS than 100 nSec. Otherwise, if TON is smaller than 100 nSec, the controller may cause problems.

Current Limit

The current limit is set by voltage developed across an external resistor on the ILIM pin. An accurate bias current flows out the ILIM pin to create a voltage across the resistor to ground. The voltage signal is heavily low pass filtered internally to avoid switching noise issues. The current limit threshold voltage is compared to the total sensed inductor current. An overcurrent condition will cause a fault condition and shutdown the PWM controller. The controller must be reset by cycling V_{CC} or the Enable input.

IMVP6 Power Good Output

Once VR_ON is activated, Vcore ramps to about Vboot. Then the first VID code is captured and a timer starts to wait for Tboot+Tcpu_up. At the end of the timing, CLK_ENABLE# is set low and Vcore is regulated to a DAC voltage determined by the VID code. When CLK_ENABLE# goes low, another timer starts and waits for Tcpu_pwrgd. At the end of the timing, IMVP6_PWRGD is set high.

At the end of the timing, the output voltage will be monitored whether it is within the Power Good Window, about +200 mV/−300 mV of the expected voltage. If yes, IMVP6_PWRGD is set high. If otherwise, IMVP6_PWRGD is set low. Then the controller must be reset by cycling V_{CC} or the Enable input.

When it is under the normal mode operation, the upper threshold will be disabled.

Overvoltage Protection
(Protection against a shorted high side MOSFET)

The output voltage is sensed via VS+ and VS− inputs and is compared to a fixed threshold of 1.7 V. If the output voltage exceeds 1.7 V, the controller shuts down immediately. If the Enable floats, the overvoltage threshold fix at 1.5 V. Then, if the output voltage exceeds 1.5 V, the controller shuts down immediately. The high side MOSFETs are shut off and the low side MOSFETs are turned on. The off/on condition is remained until power is removed from the IC or the Enable is cycled. The output voltage will be rapidly discharged. If the shorted condition persists, the fuse in the battery will be blown.

Table 3. Fault Protection Summary

Fault	Duration Before Protection	Actions	Fault Reset
Overcurrent	50 μs	TG, BG, and IMVP6_PWRGD latched low	Toggle VRONEN, VCC, VCCP1, VCCP2 or VIN
Power Good Window (+200 mV and −300 mV)	200 μs	TG, BG, and IMVP6_PWRGD latched low	Toggle VRONEN, VCC, VCCP1, VCCP2 or VIN
Overvoltage	5 μs	TG and IMVP6_PWRGD latched low BG latched high (Assume Vout should not be too negative)	Toggle VRONEN, VCC, VCCP1, VCCP2 or VIN

CONTROL LOGIC

The control logic will provide timing and sequencing for Startup, Soft−start, and Power Down.

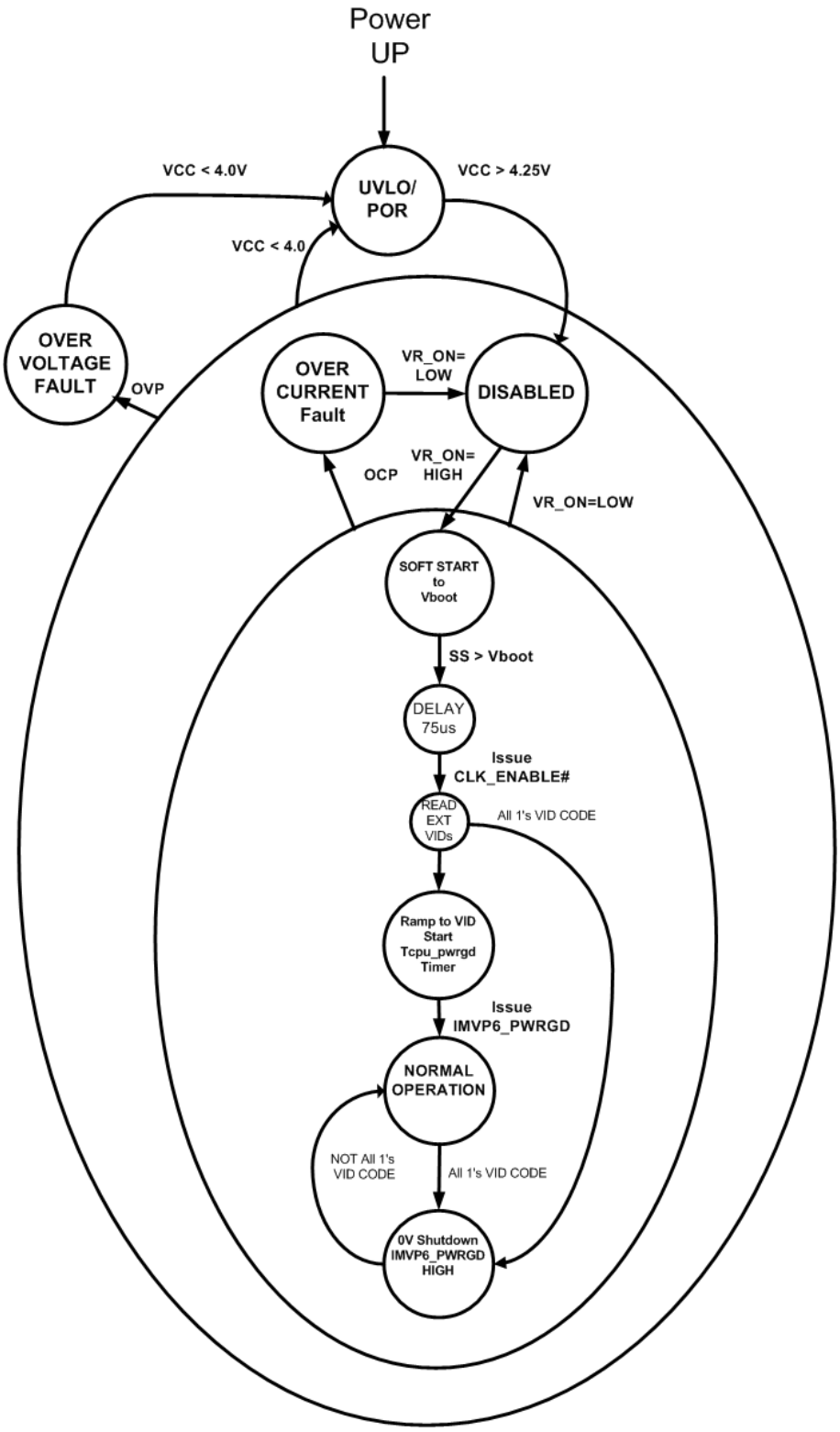


Figure 15. State Diagram

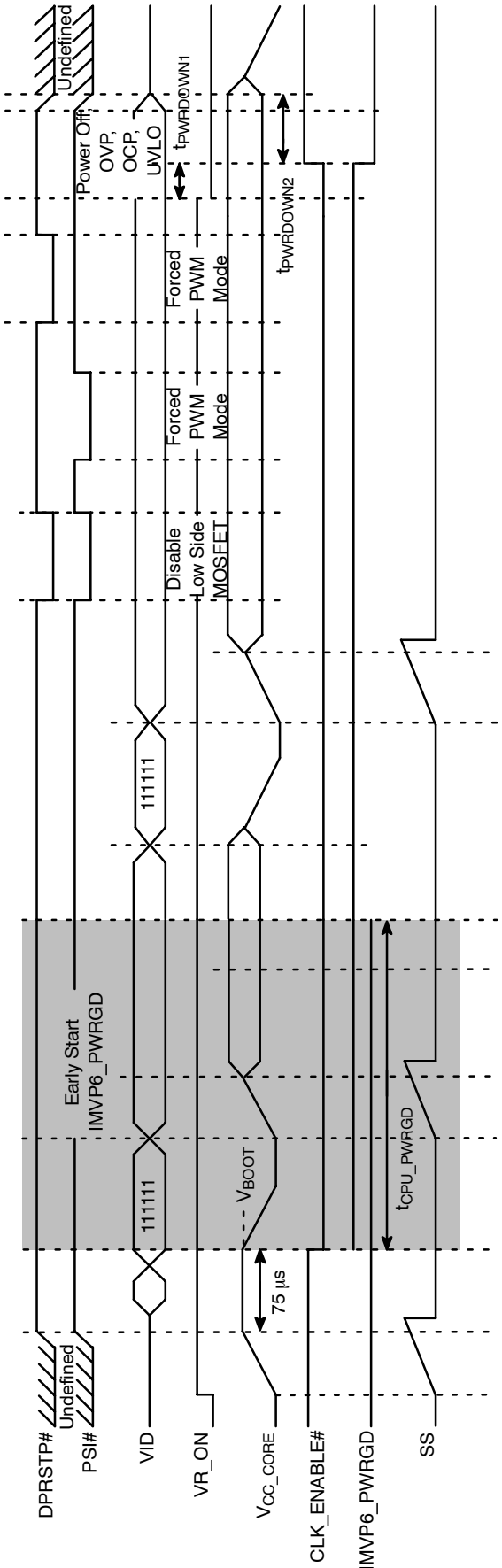
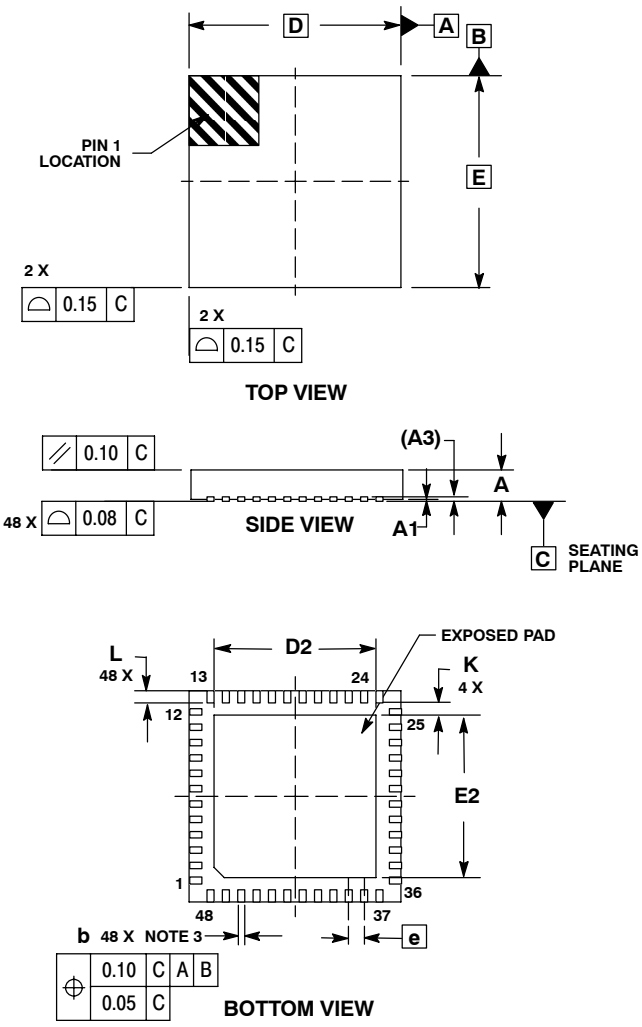


Figure 16. Complete Timing Diagram

PACKAGE DIMENSIONS

QFN48
MN SUFFIX
CASE 485K–02
ISSUE C



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		7.000 BSC	
D2	5.260	5.360	5.460
E		7.000 BSC	
E2	5.260	5.360	5.460
e		0.500 BSC	
K	0.200	----	----
L	0.300	0.400	0.500

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