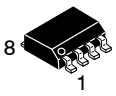
Precise CC/CV/CP Secondary-side Controller Compatible with Analog and PWM Dimming Signal

NCL38046



SOIC−8
D SUFFIX
CASE 751−07

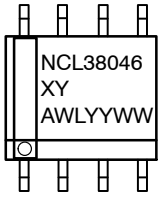
Features

- Precise CC Regulation with +/− 0.5 mV Tolerance
- Compatible with Multiple Dimming Input Signals
  - ADIM Pin Receives Analog Voltage Dimming Input
  - PWM Pin Receives PWM Duty Dimming Input
- Constant Power Regulation
- Dimming Curve Modulation
  - Maximum and Minimum Dimming Input Limit
  - Minimum Dimming Output Level Limit
  - Linear or Logarithmic Dimming Curve – Externally Selectable
- Standby Mode
- 3.3 V Reference Voltage Output
- This is a Pb−Free Device

Typical Applications

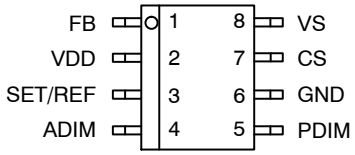
- Power Conversion
- Lighting Ballast

MARKING DIAGRAM



NCL38046	= Specific Device Code
XY	= Dimming Option
A	= Assembly Location
WL	= Wafer Lot Number
YY	= Year of Production
WW	= Work Week Number

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCL38046PADR2G	SOIC−8	2500 / Tape & Reel
NCL38046AADR2G	SOIC−8	2500 / Tape & Reel
Letter Coding L1 : P (PDIM modulation), A (ADIM modulation) L2 : Sequentially assigned from A to Z		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

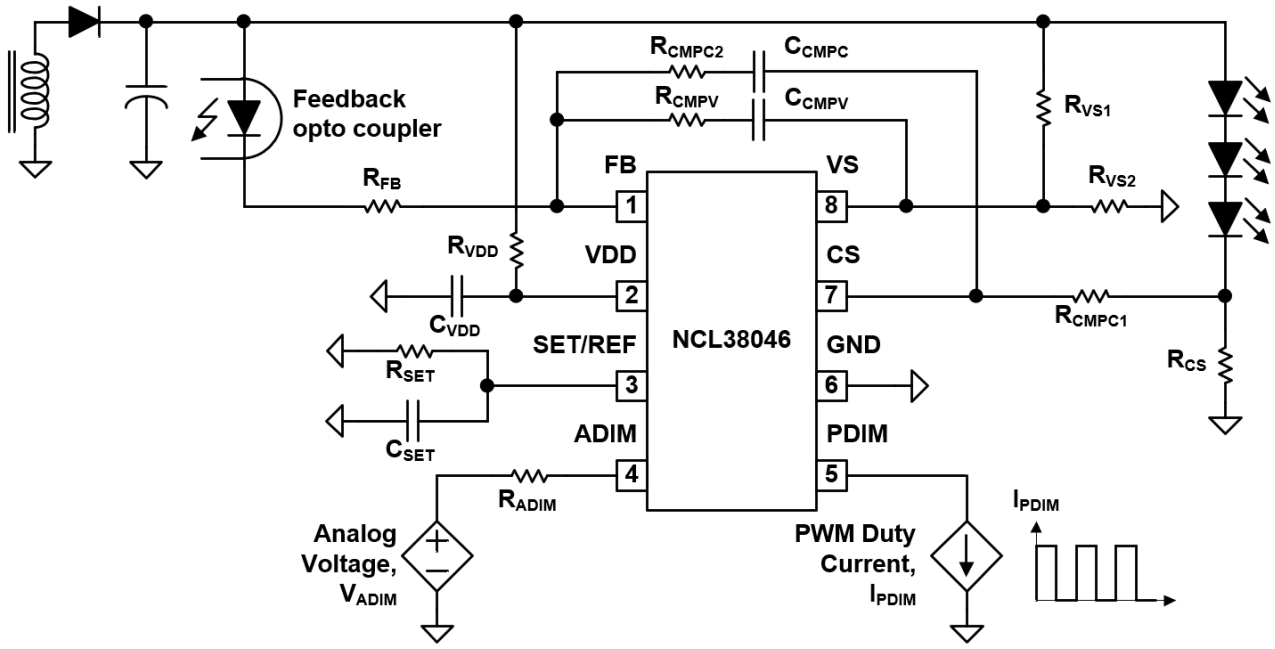


Figure 1. Application Schematic

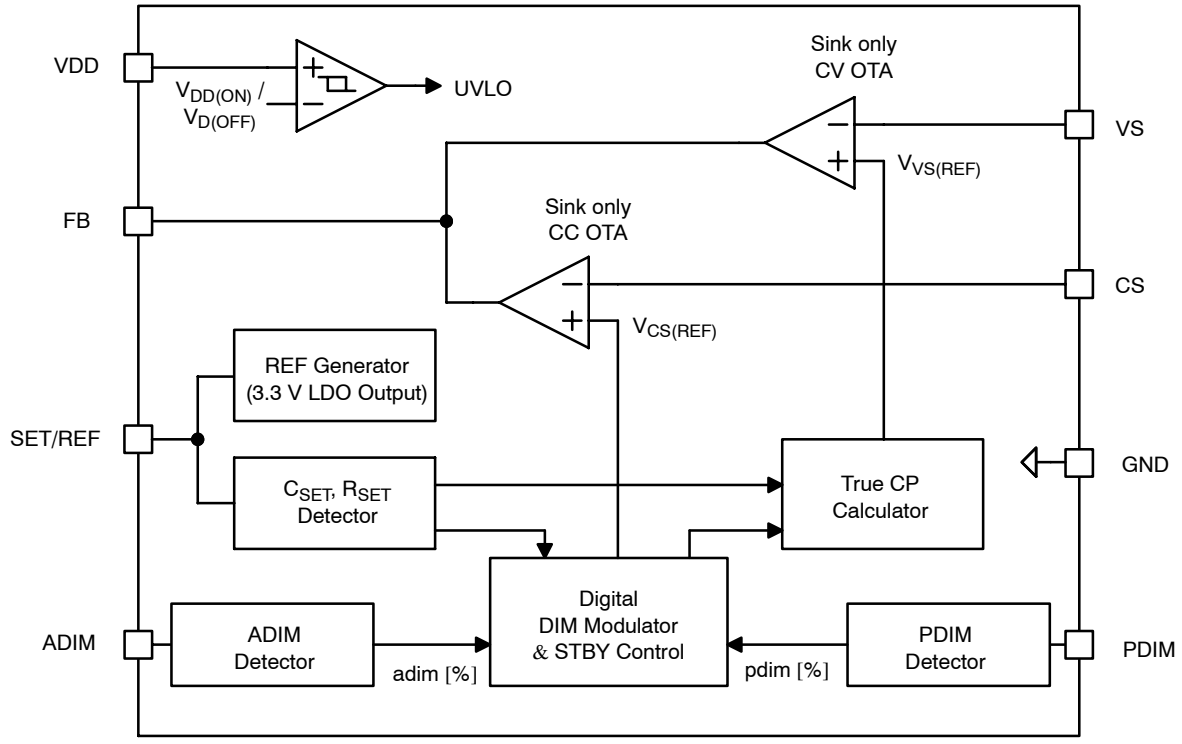


Figure 2. Simplified Block Diagram

PIN DESCRIPTION

Pin N°	Pin Name	Pin Description
1	FB	Output of the feedback OTA.
2	VDD	IC operating current is supplied to this pin
3	SET/REF	At startup, external SET resistor and capacitor are detected to adjust the internal DIM modulator parameters. Then, 3.3 V output is provided for an external use such as setting ADIM voltage.
4	ADIM	ADIM detects an analog voltage signal.
5	PDIM	PDIM detects a PWM duty current signal.
6	GND	The controller ground.
7	CS	This pin is connected to sense the output current.
8	VS	This pin is connected to sense the output voltage.

MAXIMUM RATINGS TABLE

Rating	Symbol	Value	Unit
VDD Pin Voltage Range	$V_{MV(MAX)}$	−0.3 to 30	V
FB Pin Voltage Range	$V_{FB(MAX)}$	−0.3 to VDD	V
CS, VS, ADIM, PDIM, SET/REF Pin Voltage Range	$V_{LV(MAX)}$	−0.3 to 6	V
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T	−60 to 150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb − Free Versions (Note1)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	1.5	kV
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 Thermal Resistance, Junction−to−Air	$R_{\Theta JA}$	153	°C/W

3. Mounted on a JEDEC standard 51−3 (1s0p) test board, 100 mm^2 copper area, 1 oz copper thickness

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Junction Temperature Range	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
VDD SECTION						
IC Turn−On Threshold Voltage		$V_{DD(ON)}$	8.0	8.5	9.0	V
IC Turn−Off Threshold Voltage		$V_{DD(OFF)}$	7.0	7.5	8.0	V
Startup Current	V_{DD} = 7 V	$I_{DD(ST)}$	−	−	210	μA
Operating Current	I_{PDIM} = 0 μA, R_{SET} = 9.09 kΩ (Note 4)	$I_{DD(OP-L)}$	−	0.8	1.0	mA
	I_{PDIM} = 500 μA, R_{SET} = 9.09 (Note 4)	$I_{DD(OP-H)}$	−	1.3	1.5	mA
Standby Current	PDIM = 2% in1 kHz, No R_{SET}	$I_{DD(SB)}$	400	−	600	μA
SET/REF SECTION						
SET Current		I_{SET}	47.5	50.0	52.5	μA
SET Reference Voltage	When R_{SET} = 9.1 kΩ, $V_{SET(0)} < V_{SET} < V_{SET(1)}$	$V_{SET(0)}$	281	300	319	mV
	When R_{SET} = 13 kΩ, $V_{SET(1)} < V_{SET} < V_{SET(2)}$	$V_{SET(1)}$	519	545	571	mV
	When R_{SET} = 18 kΩ, $V_{SET(2)} < V_{SET} < V_{SET(3)}$	$V_{SET(2)}$	732	765	798	mV
	When R_{SET} = 24 kΩ, $V_{SET(3)} < V_{SET} < V_{SET(4)}$	$V_{SET(3)}$	999	1040	1081	mV
	When R_{SET} = 33 kΩ, $V_{SET(4)} < V_{SET} < V_{SET(5)}$	$V_{SET(4)}$	1348	1400	1452	mV
	When R_{SET} = 43 kΩ, $V_{SET(5)} < V_{SET} < V_{SET(6)}$	$V_{SET(5)}$	1814	1880	1946	mV
	When R_{SET} = 56 kΩ, $V_{SET(6)} < V_{SET} < V_{SET(7)}$	$V_{SET(6)}$	2367	2450	2534	mV
	When R_{SET} = open, $V_{SET(7)} < V_{SET}$	$V_{SET(7)}$	3288	3400	3512	mV
SET Capacitor Detection Delay Time	Design guaranteed	$t_{SET(CAP)}$	4.76	5	5.26	μs
SET Resistor Detection Delay Time	Design guaranteed	$t_{SET(RES)}$	487	512	538	μs
REF Regulation Voltage		V_{REF}	3.26	3.30	3.34	V
PDIM and ADIM SECTION						
PDIM High Threshold Current	Increasing I_{PDIM}	$I_{PDIM(TH-H)}$	125	153	170	μA
PDIM Low Threshold Current	Decreasing I_{PDIM}	$I_{PDIM(TH-L)}$	55	70	80	μA
PDIM Maximum Current Limit	V_{PDIM} = 0 V	$I_{PDIM(MAX)}$	0.8	1	1.2	mA
PDIM Regulation Voltage	I_{PDIM} = 250 μA	V_{PDIM}	2.9	3.0	3.1	V
PDIM Minimum Frequency Limit	Design Guaranteed	$f_{PDIM(MIN)}$	65	−	−	Hz
ADIM Maximum Voltage		$V_{ADIM(MAX)}$	2.47	2.50	2.53	V
VS SECTION						
VS OTA Input Offset		$V_{VS(OTA-IO)}$	−25	0	+25	mV
VS Maximum Regulation Voltage		$V_{VS(REG-MAX)}$	2.425	2.500	2.575	V
VS Standby Regulation Voltage	$D_{PDIM} < D_{PDIM(SB-EN)}$ in PA version $V_{ADIM} < V_{ADIM(SB-EN)}$ in AA version	$V_{VS(REG-SB)}$	0.475	0.500	0.525	V
CS SECTION						
CS OTA Input Offset	Temp range: −40°C ~ 125°C	$V_{CS(OTA-IO)}$	−0.8	0	0.8	mV
	Temp range: −40°C ~ 85°C		−0.45	0	0.45	mV
	Only 25°C		−0.175	0	0.175	mV
CS Maximum Regulation Voltage	I_{FB} = 0.5 mA in a closed loop regulation Temp range: −40°C ~ 125°C	$V_{CS(REG-MAX)}$	98	100	102	mV
	I_{FB} = 0.5 mA in a closed loop regulation Temp range: 25°C ~ 85°C		99	100	101	mV

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to 125°C, unless otherwise noted) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
CS Half Regulation Voltage	I_{FB} = 0.5 mA in a closed loop regulation Temp range: −40°C ~ 125°C (Note 5)	$V_{CS(REG-HALF)}$	49.5	50.5	51.5	mV
	I_{FB} = 0.5 mA in a closed loop regulation Temp range: 25°C ~ 85°C (Note 5)		50	50.5	51	mV
CS Minimum Regulation Voltage	I_{FB} = 0.5 mA in a closed loop regulation Temp range: −40°C ~ 125°C	$V_{CS(REG-MIN)}$	0.3	1	1.7	mV
	I_{FB} = 0.5 mA in a closed loop regulation Temp range: 25°C ~ 85°C		0.6	1	1.4	mV
CS Fault Current		$I_{CS(FAULT)}$	−28	−24	−19	μA
FB SECTION						
FB Maximum Sink Current of CS OTA	V_{CS} = 1 V	$I_{FB(SINK-CS-MAX)}$	2.5	–	–	mA
FB Maximum Sink Current of VS OTA	V_{VS} = 3 V	$I_{FB(SINK-VS-MAX)}$	2.5	–	–	mA
Transconductance of CS OTA		$g_{M(CS)}$	–	7	–	mho
Transconductance of VS OTA		$g_{M(VS)}$	–	3	–	mho

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. I_{DD} is affected to R_{SET} value. If you want to know I_{DD} with other R_{SET}, $I_{DD(RSET\ changed)} = I_{DD} - 3.3\,V \cdot \left(\frac{1}{9.09k} + \frac{1}{RSET}\right)$
5. The value has an offset due to $MOD_{OUT(MIN)}$ to modulate a dimming curve. $V_{CS(REG)}$ is calculated as shown below.

$$V_{CS(REG)} = Dim[\%] \cdot slope + off\,set \text{ , where } slope = \frac{MOD_{OUT(MAX)} - MOD_{OUT(MIN)}}{MOD_{IN(MAX)} - MOD_{IN(MIN)}},\ off\,set = MOD_{OUT(MAX)} - slope \cdot MOD_{IN(MAX)}$$

APPLICATION INFORMATION

NCL38046 performs precise CC regulation in the wide dimming range controlled by both PWM duty and analog voltage signal. Dimming curve is internally modulated by an effective dimming input range (e.g., 10% ~ 90%) and the minimum dimming output level (e.g., 1%). Also, either linear or logarithmic dimming curve is externally selected by a SET capacitor. Constant power regulation is implemented by CV regulation reference defined inversely proportional to the dimming level where the CP level is flexibly set by an external SET resistor.

CC/ CV Regulation

For high CC accuracy, an input voltage offset of the CC regulation OTA is significantly reduced by a novel amplifier design with high resolution trimming so that the input voltage at room temperature is less than +/− 0.1 mV. When a LED load is connected, CS pin voltage (V_{CS}) is regulated to $V_{CS(REF)}$, an internally generated CS reference voltage controlled by PDIM and ADIM inputs. When the LED load is open, V_{CS} drops to 0 V and CC OTA does not sink FB current and V_{VS} is regulated to $V_{VS(REF)}$.

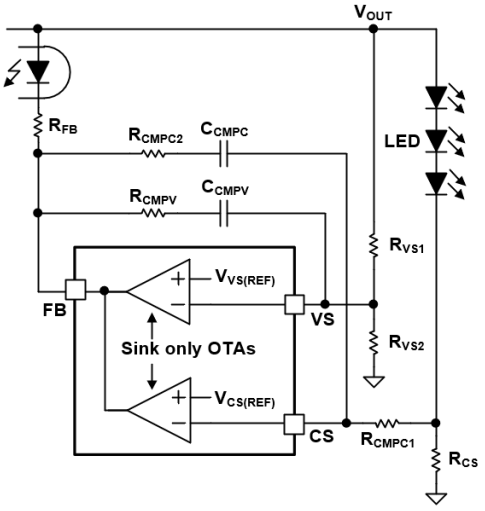


Figure 3. CC/CV Regulation Block

CC/ CV Regulation

PDIM and ADIM Detection

As shown in Figure 4, PDIM pin voltage is regulated to 3 V by the pull−up buffer. PDIM current, I_{PDIM}, is compared with $I_{PDIM(TH-H/L)}$ hysteretic current thresholds and the comparison output signal is converted to pdim signal (0% ~ 100%) by the duty extractor. When I_{PDIM} is higher than the current threshold, it is considered as the on state in the PWM duty. The recommended I_{PDIM} on−state level is 300 ~ 600 μA and PDIM pin is pulled down to 0 V when I_{PDIM} is higher than 1 mA in order to limit the VDD operating current. 200 Hz PWM frequency is recommended to perform high resolution dimming.

ADIM signal is detected by the ADIM voltage detector and ADIM voltage input range is 0 ~ 2.5 V. The detected ADIM voltage is converted to adim signal (0% ~ 100%). At startup, ADIM pin is buffered by SET/REF pin voltage as described in Section. *REF Function*. So, 10 kΩ R_{ADIM} in Figure 4 is recommended when V_{ADIM} is set by the external voltage source not to conflict with an internal buffer (SET/ref to ADIM) output.

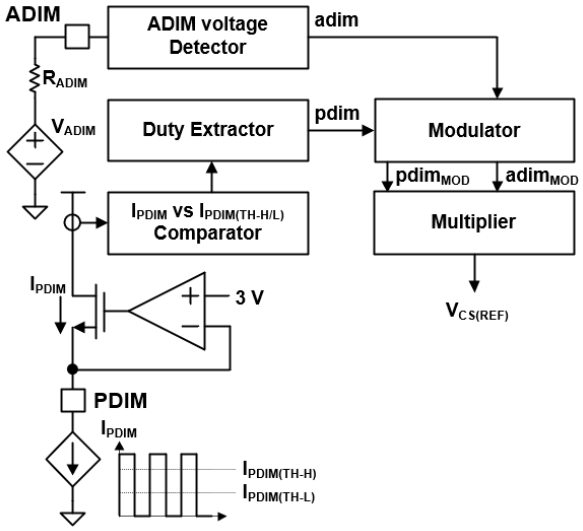


Figure 4. CC Reference Generation Block

Dimming Signal Modulation

In general, an external dimming signal generator such as 0 − 10 V dimmer doesn't provide the full range of the dimming signal. In such case, NCL38046 can scale either pdim or adim signal by the internal modulator. As shown in Figure 5, the modulator input signal, mod_{IN}, has an effective input range between 10% and 90%. In other words, when mod_{IN} is 10%, mod_{OUT} becomes the min value and mod_{OUT} doesn't decrease although mod_{IN} goes below 10% because mod_{OUT} is clamped to 1% by $mod_{OUT(MIN)}$. When mod_{IN} is lower than 3%, NCL38046 enters STBY. In order to exist STBY, mod_{IN} should be higher than 5% because of STBY threshold hysteresis.

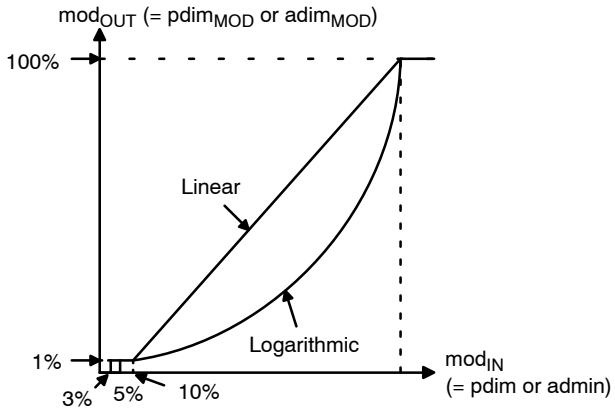


Figure 5. Dimming Signal Modulation

When mod_{IN} is 90%, mod_{OUT} becomes the max value and mod_{OUT} doesn't increase even though mod_{IN} rises above 90% by $mod_{IN(MAX)}$.

There're also two types of dimming curves (Linear and Logarithmic).

Multiplier

Recently, LED drivers generally control the output current by the dual dimming signals to set the maximum output current and to implement the dimming function. In order to perform the multiple dimming in NCL38046, adim (0 ~ 100%) and pdim (0 ~ 100%) signals are multiplied and scaled to $V_{CS(REF-MAX)}$ to provide $V_{CS(REF)}$ as shown in Figure 6 and Figure 7. The dimming signal input is usually modulated, and the maximum output current setting signal is not modulated just to set the coefficient in the dimming curve.

When analog voltage signal at ADIM is used for the maximum output current setting and PWM duty signal at PDIM is used for dimming, PA version should be used. $V_{CS(REF)}$ is determined by (eq. 1) which corresponds to Figure 6.

$$V_{CS(REF)}[V] = V_{CS(REF-MAX)}[V] \cdot adim[\%] \cdot pdim_{MOD}[\%] \quad \text{(eq. 1)}$$

When adim is used for dimming and pdim is to set the maximum output current, AA version should be used. $V_{CS(REF)}$ is set by (eq. 2) corresponding to Figure 7.

$$V_{CS(REF)}[V] = V_{CS(REF-MAX)}[V] \cdot pdim[\%] \cdot adim_{MOD}[\%] \quad \text{(eq. 2)}$$

$V_{CS(REF)}$ dimming voltage range is limited by $V_{CS(REF-MAX)}$ and $V_{CS(REF-MIN)}$.

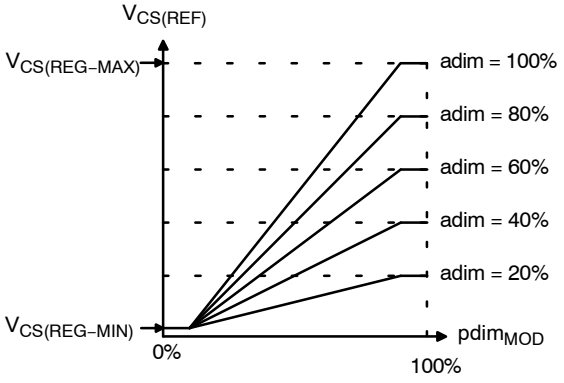


Figure 6. Dimming Curve in PA Version

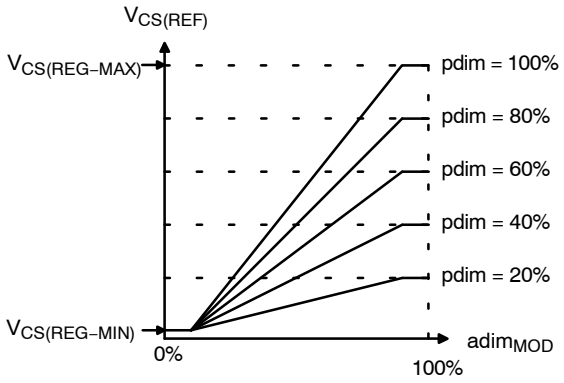


Figure 7. Dimming Curve in AA Version

CV Reference

Constant voltage reference is determined by constant power regulation block to protect the LED load and limit the LED driver power when maximum output current is incorrectly set. CV reference, $V_{VS(REF)}$, is determined by:

$$V_{VS(REF)}[V] = 2.5\ V \cdot K_{CP}[\%] / dim_{CP}[\%] \quad \text{(eq. 3)}$$

where $K_{CP}[\%]$ is a constant power coefficient and $dim_{CP}[\%]$ is CP dim input which is adim in PA version or pdim in AA version. K_{CP} is set by R_{SET} value as described in Section. *SET/REF Function*. Also, $V_{VS(REF-MAX)}$ is clamped to 2.5 V.

Figure 8 shows an example of the load operating point assuming that the maximum current spec of an LED load is at 50% $V_{CS(REF-MAX)}$ by setting adim at 50% (V_{ADIM} = 1.25 V) and the output current dimming is controlled by $pdim_{MOD}$.

Without CP function, the LED current will be twice than its maximum current rating with the LED damage if adim is mistakenly set to 100% (V_{ADIM} = 2.5 V).

With CP function in Figure 8, $V_{VS(REF)}$ is set by (eq. 3) and the LED load is safe even though adim is wrongly set to 100% because $V_{VS(REF)}$, inversely proportional to adim, is set lower than the max load operating point. If adim is correctly set back to 50%, $V_{VS(REF)}$ is set higher than the max load condition and the LED load current is regulated to the right max load condition by CS regulation.

When the LED load is open, the output voltage is regulated little higher than the LED load forward voltage so that there won't be a large inrush current from the output capacitor to the LED load when the LED load is connected again. In the conventional LED driver with CP function, CV regulation level is determined by total LED current level so that the output voltage is regulated to the maximum output level at LED open condition. In such condition, the LED load can be damaged when the LED load is connected because the output regulation level is much higher than the LED load forward voltage.

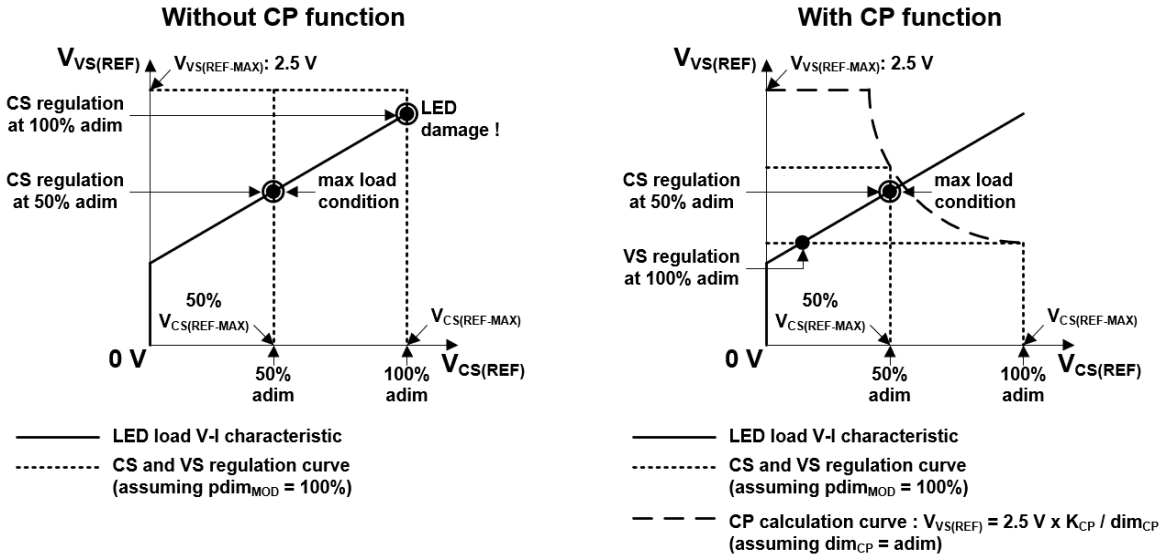


Figure 8. Operating Point by the Maximum Output Current Set Level

Standby Mode

When either adim or pdim is lower than a standby threshold level which is PDIM = 3% in PA version or V_{ADIM} = 75 mV in AA version, the CC OTA is disabled to terminate the output current regulation and CV OTA reference, $V_{VS(REF)}$, is changed to $V_{VS(REG-SB)}$ to turn off the LED load during standby mode.

SET/REF Function

SET and REF Sequence

NCL38046 has a multi−functional pin, VSET/REF, for setting internal parameters and providing 3.3 V reference output for the external use.

As shown in Figure 9, $V_{SET/REF}$ is pulled down to 0 V for 64 μs once V_{DD} is higher than $V_{DD(ON)}$. Then, SET/REF pin is pulled up by 50 μA I_{SET}. If $V_{SET/REF}$ is lower than $V_{SET(0)}$ due to C_{SET} after 5 μs $t_{SET(CAP)}$ delay, C_{SET} connection is detected. If $V_{SET/REF}$ is higher than $V_{SET(0)}$, NCL38046 decides that C_{SET} is not connected. For C_{SET} detection, 1.2 nF is used.

After C_{SET} detection, NCL38046 waits for R_{SET} detection for 512 μs $t_{SET(RES)}$ delay until $V_{SET/REF}$ level is settled to R_{SET} x I_{SET}, then $V_{SET/REF}$ is compared with internal references, $V_{SET(n)}$ (n = 0 ~ 7). For R_{SET} detection, 9.1 / 13 / 18 / 24 / 33 / 43 / 56 kΩ is used as shown in Table 1.

If SET/REF pin is open or short circuited, $V_{SET/REF}$ will be higher than $V_{SET(7)}$ or lower than $V_{SET(0)}$. In such case, $V_{SET/REF}$ reset (S_{RST} high period) and I_{SET} enabling time (S_{SET} high period) in Figure 9 are repeated and FB pin voltage is slowly pulled down to reduce the power delivery to the load until R_{SET} is normally detected.

Once C_{SET} and R_{SET} detections are completed, $V_{SET/REF}$ is regulated to 3.3 V by internal LDO, and the 3.3 V reference voltage can be utilized for various purpose in the external circuit.

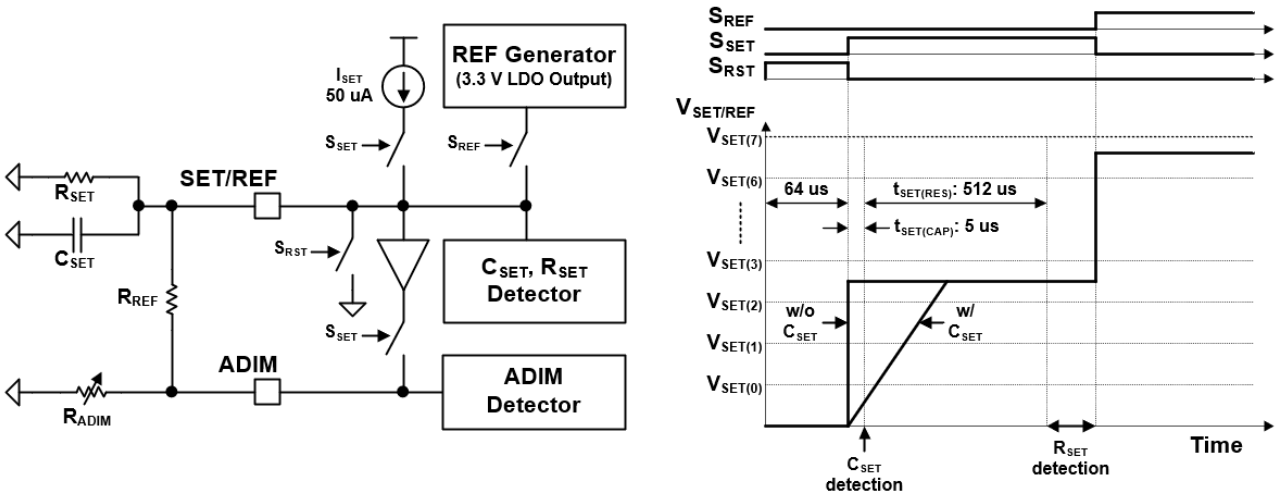


Figure 9. SET/REF Functional Block and Sequence

Table 1. COMPONENTS AT SET FUNCTION

R_{SET}	K_{CP}
9.1 kΩ	40%
13 kΩ	50%
18 kΩ	60%
24 kΩ	70%
33 kΩ	80%
43 kΩ	90%
56 kΩ	100%
C_{SET}	**Dimming curve**
0 nF	Linear
1.2 nF	Logarithmic

REF Function

After C_{SET} and R_{SET} detection, SET/REF pin voltage is regulated to 3.3 V. The reference voltage can be utilized to set ADIM voltage by adding R_{REF} resistor between SET/REF and ADIM pin so that ADIM voltage, V_{ADIM}, is determined by:

$$V_{ADIM}[V] = 3.3\ V \cdot R_{ADIM}/(R_{REF} + R_{ADIM}) \quad \text{(eq. 4)}$$

Variable resistor can be used for R_{ADIM} to externally adjust the maximum output current level by ADIM.

During I_{SET} enabling time (S_{SET} high period), R_{REF} network can affect R_{SET} detection level. In order to monitor only R_{SET} impedance through SET/REF pin, ADIM pin voltage is buffered same as SET/REF pin voltage and R_{REF} impedance from SET/REF pin becomes infinite with no effect on the SET/REF voltage.

Table 2. NCL38046 OPTION TABBLE

P/N	1st Letter	2nd Letter	MOD Input	STBY Trigger	$V_{CS(REF-MAX)}$	$V_{CS(REF-MIN)}$	$V_{VS(REF-SB)}$	R_{SET} func.	K_{CP}
NCL38046	P	A	a1	b1	c2	d3	e2	f1	g22 (69%)
	A	A	a2	b2	c2	d3	e2	f1	g22 (69%)

P/N	1st Letter	2nd Letter	CP_sel	$MOD_{IN(MIN)}$	STBY Threshold	$MOD_{IN(MAX)}$	$MOD_{OUT(MIN)}$	Log. Curve Eq.
NCL38046	P	A	h1	i2	j2	k2	l5	m1
	A	A	h2	i2	j2	k2	l5	m1

MOD Input

a1	pdim
a2	adim

CP dim input (dim_{CP})

h1	adim
h2	pdim

STBY Trigger

b1	pdim
b2	adim

$MOD_{IN(MIN)}$

i1	0%
i2	10%

$V_{CS(REF-MAX)}$

c1	50 mV
c2	100 mV
c3	200 mV
c4	500 mV

STBY threshold

j1	6% / 8%
j2	3% / 5%
j3	2% / 3%
j4	Disabled

$V_{CS(REF-MIN)}$

d1	0%
d2	0.4%
d3	1%
d4	2%

$MOD_{IN(MAX)}$

k1	100%
k2	90%
k3	85%
k4	80%

$V_{VS(REF-SB)}$

e1	0 V
e2	0.5 V
e3	1 V
e4	1.5 V

$MOD_{OUT(MIN)}$

l1	10%
l2	7.5%
l3	5%
l4	2%
l5	1%

R_{SET} Function

f1	K_{CP} set
f2	$MOD_{OUT(MIN)}$ set

Logarithmic Curve Equation

m1	modout = modin^2
m2	modout = modin^3

K_{CP}

g1 ~ g32	100% ~ 3% (3% step)

PCB LAYOUT GUIDANCE

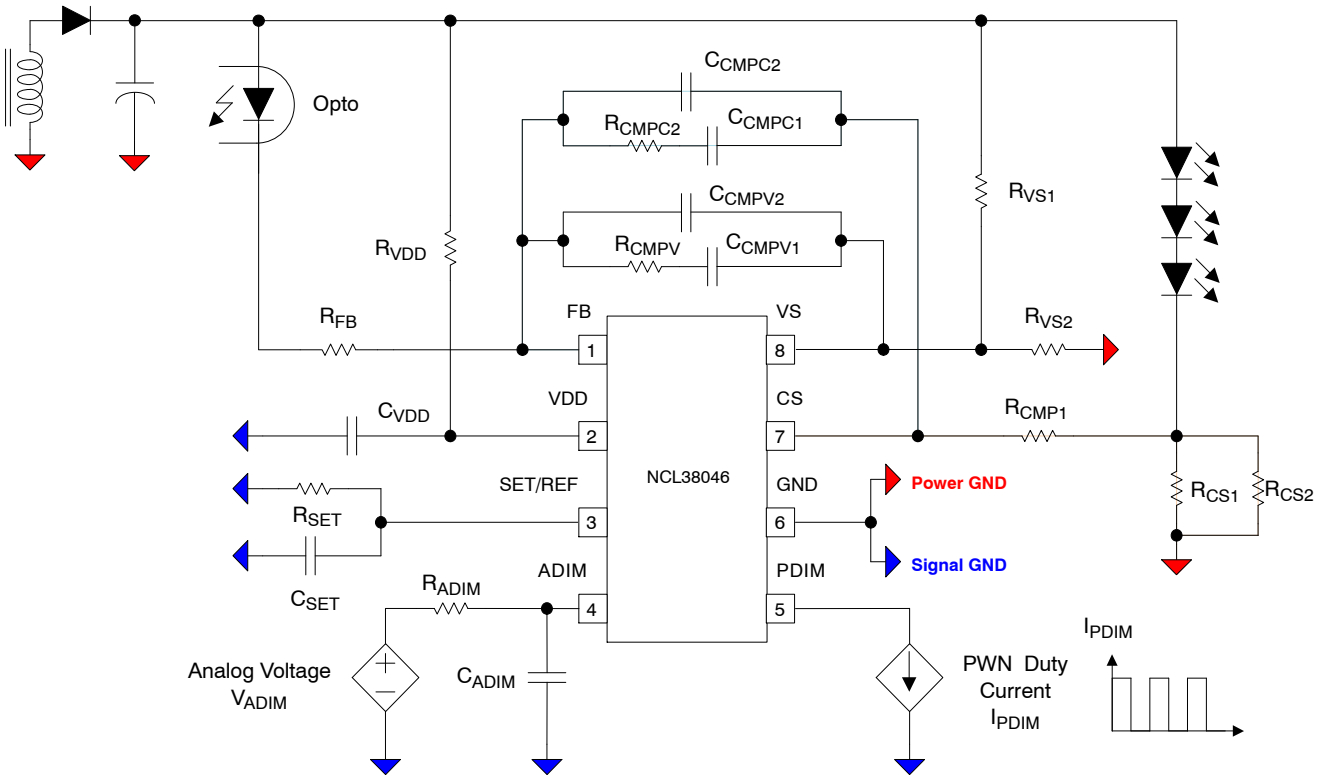


Figure 10. NCL38046 Schematic

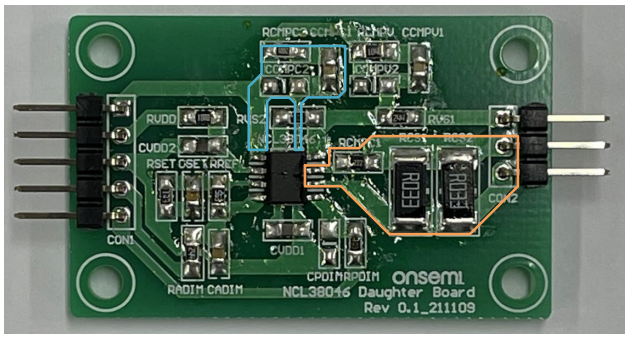


Figure 11. NCL38046 Daughter Board

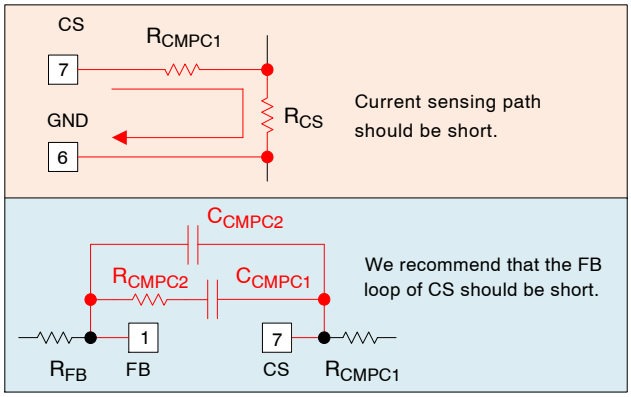


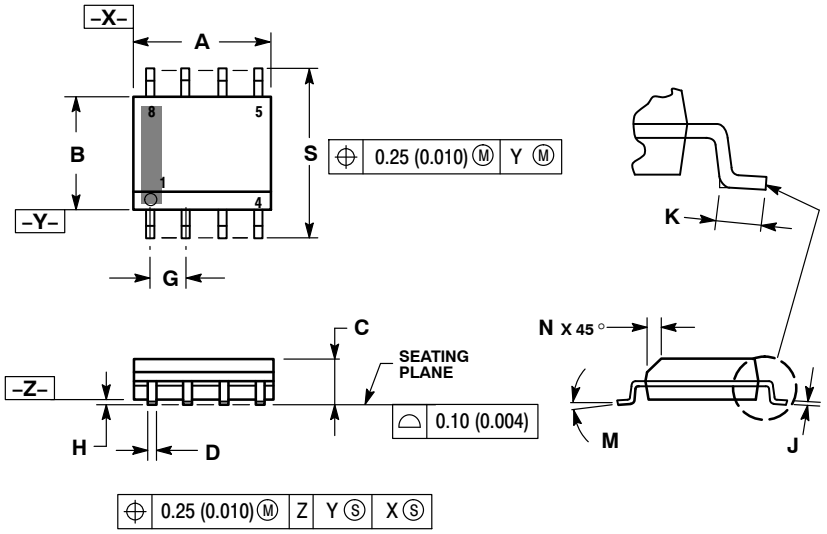
Figure 12. NCL38046 Layout Guidance

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

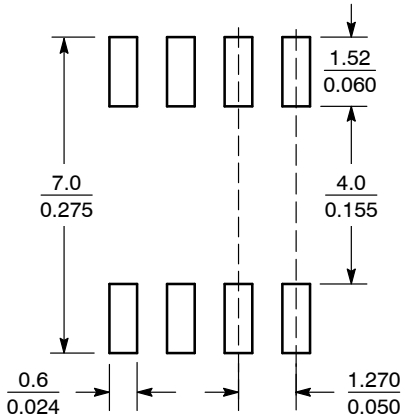
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

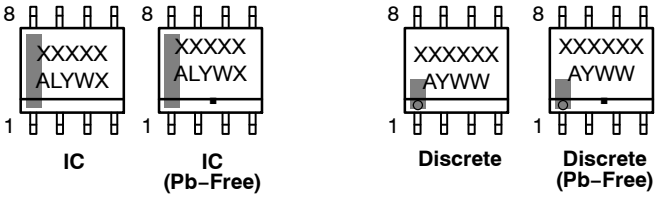
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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