onsemi Device Nomenclature

TND310

This document contains the device nomenclature breakdown (also referred to as the part number decoder, product naming convention, or part naming convention) for **onsemi** orderable devices. Whenever possible, **onsemi** uses these numbering systems in the naming of their products.

The ESD/TVS, small signal diode and transistor, and thyristor portfolios have no single standard naming convention. They consist of many industry standard nomenclatures, along with several market targeted naming conventions. For any questions, please contact your local **onsemi** sales representative.

Historical Nomenclature Notes

During its history, **onsemi** has been part of another company, and has acquired other companies and product lines. In order to maintain consistency for customers, part numbers have not changed, wherever possible. The following prefixes may indicate the original manufacturer:

Ax – Aptina Imaging Corporation

AX – Axsem AG

ADx – Analog Devices, Inc.

AMIS – AMI Semiconductor

ASM – PulseCore

CAT – Catalyst Semiconductor

CS – Cherry Semiconductor

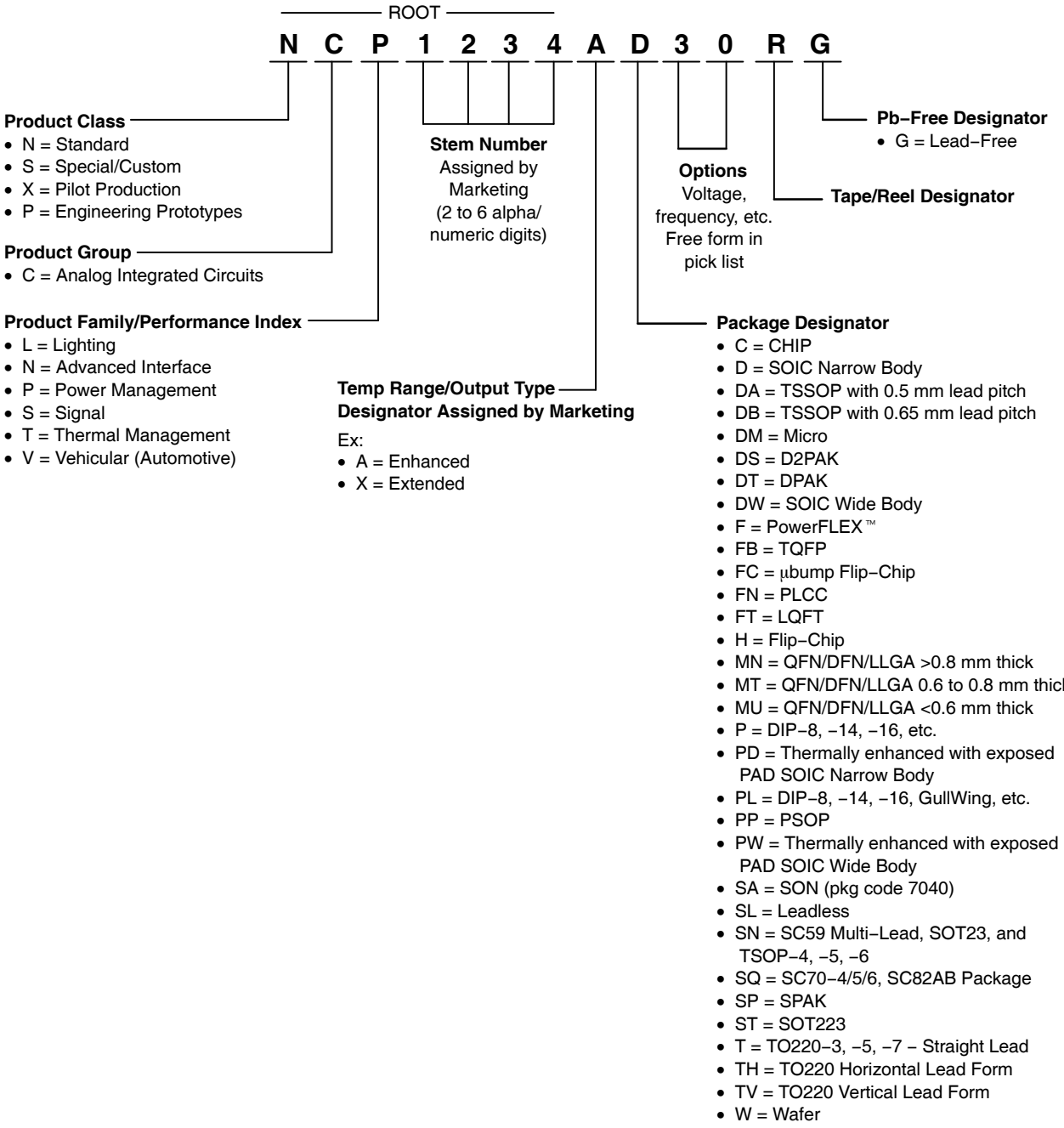
Kxx – Truesense Imaging, Inc.

MC – Motorola

NOI – Cypress Semiconductor

Current Nomenclatures

Naming Convention for Analog Devices



Naming Convention for CMOS Logic Family Devices

MC 74 VHCT WW XXXXX Y Z R2 G

Circuit Identifier
- MC = Motorola
- NL = **onsemi**

Family Type
- 74 = 74 Series
- AS = Analog Switch
- SF = Special Function
- 17 = Single Gate
- 27 = Dual Gate
- 37 = Triple Gate

CMOS Specification Identifier
- AC = Advance CMOS
- ACT = Advance CMOS TTL Compatible
- HC = Buffered High Speed CMOS
- HCT = High Speed CMOS TTL Compatible
- HCU = Unbuffered High Speed CMOS
- LCX = Low Voltage CMOS
- LVX = Low Voltage CMOS
- VCX = High Speed, Low Voltage CMOS
- VHC = Advanced High Speed CMOS
- VHCT = VHC TTL Compatible
- SV = Ultra Low Voltage Single Gate (VCX)
- SZ = Single Gate LCX
- WZ = Double/Triple Gate LCX

Special Feature
- Blank = No Specific Feature
- H = Bus Hold
- 1G = Single Gate
- 1GT = Single Gate TTL
- 2G = Dual Gate
- 2GT = Dual Gate TTL
- 3G = Triple Gate
- 3GT = Triple Gate TTL

Function Type
- 2 to 5 Characters

Package Type
- D = 150 mil SOIC
- DW = 300 mil SOIC
- DT = TSSOP
- DF = SC-88, SC-88A
- DBV = SC-74, SC-74A
- US = US-8
- P5 = SOT-9
- XV = SOT-5
- MN = QFN >0.8 mm Thick (Nom)
- MT = QFN 0.7 mm Thick (Nom)
- MQ = QFN 0.4 or 0.5 mm Thick (Nom)
- MU = DFN 0.4 or 0.5 mm Thick (Nom)
- MX = XFN or DFN 0.3 mm Thick (Nom)

Pin Pitch
- Blank = Not Specified
- 1 = 0.5 mm
- 2 = 0.4 mm
- 3 = 0.3 mm

Tape/Reel Designator

Pb−Free Designator
- G = Lead−Free

Naming Convention for Analog Switch Devices

NLAS 5 2 2 3 0

Application Type
- 5 = Audio
- 7 = Multimedia/USB/Data
- 9 = General Purpose

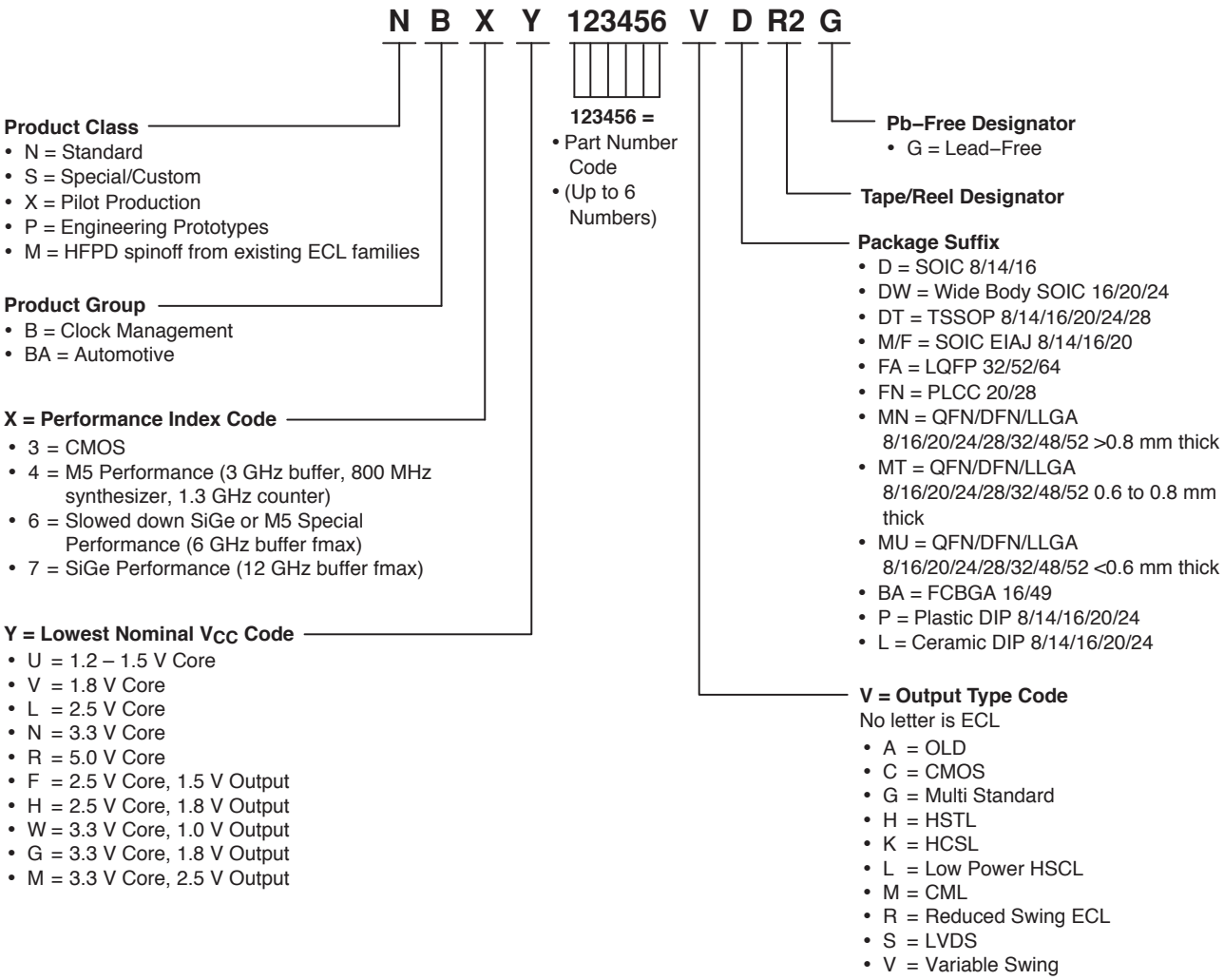
Channel Number
- 1, 2, 3, 4, 8...

Function Number
- 1 = SPST
- 2 = SPDT
- 3 = DPDT
- 4 = 4:1 Multiplexer
- 8 = 8:1 Multiplexer

Ron Range
- 0: Ron<100 ~ 1000 Ω
- 1: Ron<10 ~ 100 Ω
- 2: Ron<1 ~ 10 Ω
- 3: Ron<1 ~ 0.5 Ω

Flexible
(Could be used for bandwidth or other parameters) Will not be present unless needed.

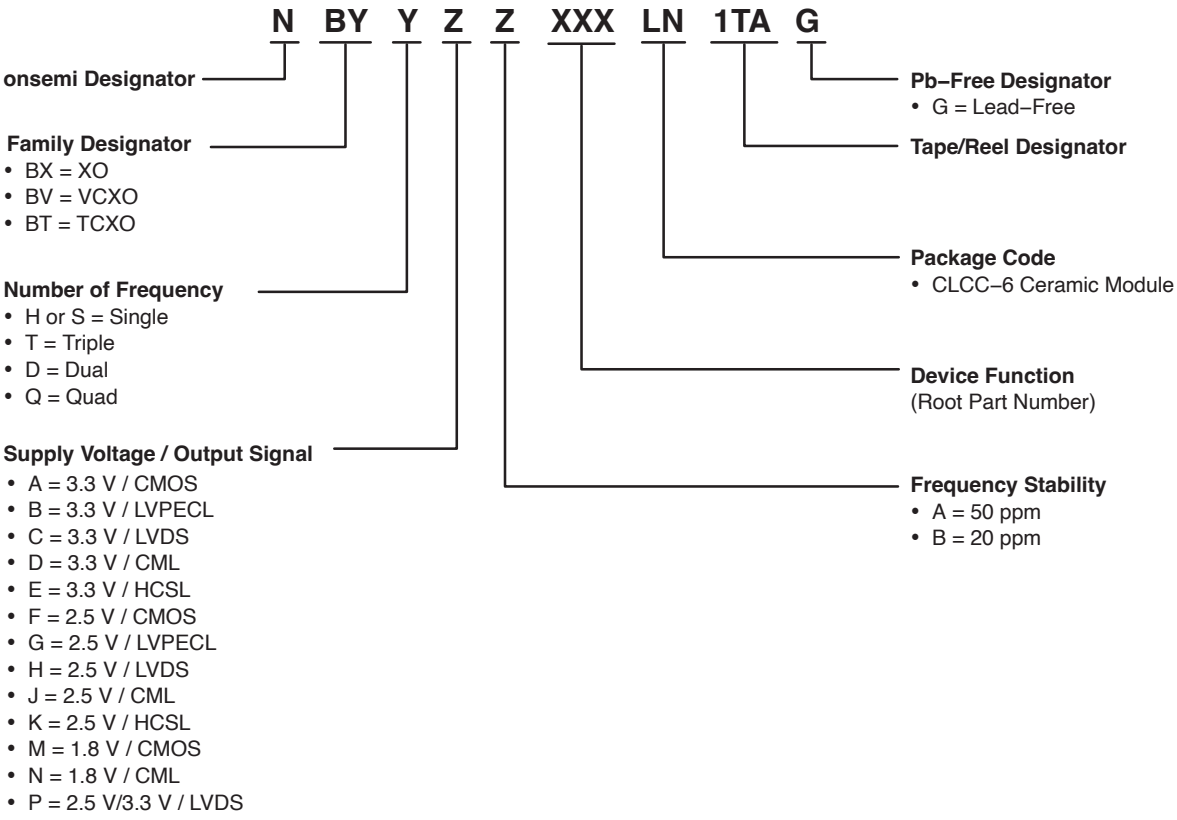
Naming Convention for Clock and Data Management Devices



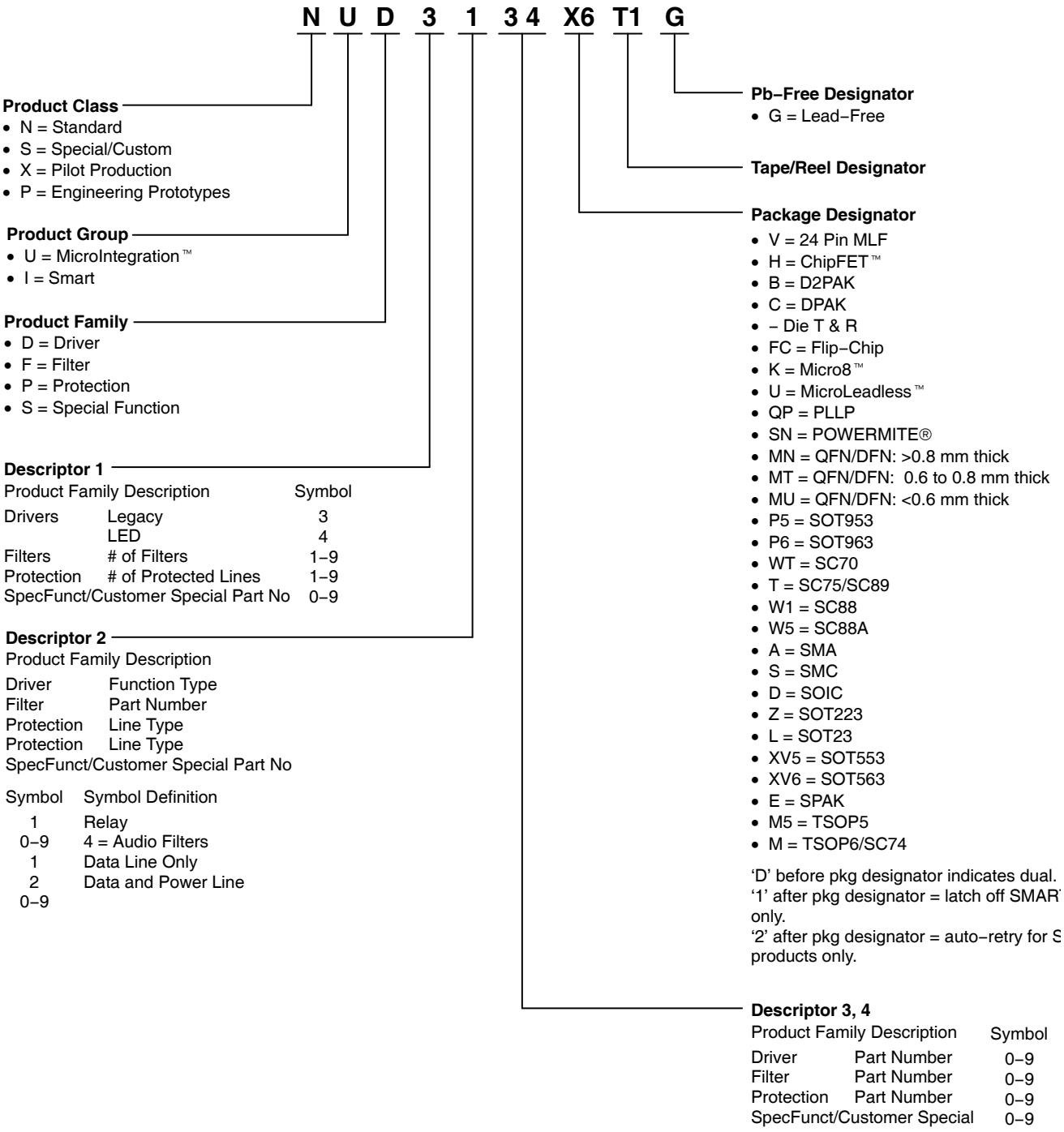
Possible Device Prefixes

MC	MCH	MCK	MCW (Prescaler & Wafer Sales)
MCWh	MCWK	NBC	NBSG
SB	SC	NBSX (Mixed Signal)	

Naming Convention for Crystal Oscillator Devices



Naming Convention for Integrated Solutions Devices



Naming Convention for MOS Power Devices

N G MS 1 3 001 N T1 G

Product Class
- N = Standard
- S = Special/Custom
- X = Pilot Production
- P = Engineering Prototypes

Product Group
- G = IGBT
- M = Micro Integration
- T = Power MOSFETs
- V = Automotive MOSFETs

Package Designator(s)
- A = SC-75
- B = D2PAK
- C = Chip Sales
- D = DPAK
- E = SC-89
- F = SOT-223 (Low Voltage)
- F = TO-220FP (High Voltage)
- G = TSOP
- H = ChipFET™
- J = SC-88
- K = SOT-723
- L = QFN/DFN/WDFN
- M = SOIC-8
- N = SOT-1123/SOT-553/XDFN/ULLGA
- P = TO-220
- Q = 8 mm x 8 mm (Low Voltage)
- Q = TSSOP (High Voltage)
- R = SOT-23
- S = SC-70
- T = Micro8™ (Low Voltage)
- T = SOT-223 (High Voltage)
- U = SOT-953
- V = FlipChip
- W = TO-247
- Y = TO-264
- Z = SOT-563
- AT = ATPAK
- BA = TO-263 FA Forming
- BD = TO-263 FD Forming
- CR = Dicing Ring Packing
- CT = Wafer Tray Packing
- CW = Wafer Packing
- DP = TP
- FP = TO-220F-3FS/3SG
- PL = TO-220-3L
- TL = TO-3P
- UL = TO-3PF
- WL = TO-247-3L
- P3 = CP
- P4 = CP4
- C3 = CPH3
- C5 = CPH5
- C6 = CPH6
- EC = ECH8
- EF = EFCP
- EM = EMH8
- M3 = MCPH3
- M5 = MCPH5
- M6 = MCPH6
- PC = PCP
- SC = SCH6
- FW = SOIC8
- VE = VEC8
- 'D' = After Package Designator = Dual
- 'L' = After Package Designator = Leadless
- 'S' = After Package Designator = Single Config
- 'F' = After Package Designator = Flat Lead (or Legacy FULLPAK™)
- 'G' = After Package Designator = >0.80 mm Thick
- 'J' = After Package Designator = 0.60 to 0.80 mm Thick
- 'Q' = After Package Designator = Quad
- 'U' = After Package Designator = <0.60 mm Thick

Battery Protection Products
- EFC = EFCP (CSP)
- EMH = EMH8
- ECH = ECH8

Voltage Rating
- 1 = <1 to 8 V
- 2 = 9 to 12 V
- 3 = 13 to 20 V
- 4 = 21 to 30 V
- 5 = 31 to 60 V
- 6 = 61 to 124 V
- 7 = 125 to 250 V
- 8 = 251 to 499 V
- 9 = 500 V +

Technology
- 0 = HD Plus
- 1 = Trench 1
- 2 = Standard IGBT
- 3 = Smart IGBT
- 4 = HD3E
- 5 = Raised Poly
- 6 = TMOS 7
- 7 = FastMOS
- 8 = Trench 2
- 9 = Trench 3
- A = Trench 4
- B = Trench 5
- C = Trench 6
- D = Superjunction 2
- E = SSG Trench 4
- F = SSG Trench 5
- G = GaN
- H = Trench 8
- J = Trench 7
- L = Trench 10
- P = SSG HVFET
- R = RF MOSFET
- U = UH4
- U1 = Superjunction Gen 1
- U2 = Superjunction Gen 2

Part Number
- (000 - 999) Sequential

Polarity/Other
- A = Current Sense
- B = Bidirectional
- N = N Channel
- P = P Channel
- C = Complementary
- F = FETKY®
- K = Temperature Sense
- L = Low Logic Level
- U = Low Gate Drive (Under 2.5 V)
- S = SenseFET
- T = TVS
- W= Wafer Pack
- Z = ESD
- E = Enhanced

Packaging/Tape & Reel Designator

Pb-Free/Halide Free Designator
- G = Pb-Free Plating/260c
- H = Halide Free Compound

Naming Convention for SO-8 (MiniMOS), Micro8, SOT-223, and TSOP-6 Power MOSFETs

PREVIOUS FORMAT 1

M M SF 4 P 01 HD R1

Circuit Identifier

TMOS®
- M = Miniature

Package Type
- DF = Dual FET (SO−8)
- SF = Single FET (SO−8)
- FT = FET Transistor (SOT−223)
- MTSF = Single FET (Micro8)
- MTDF = Dual FET (Micro8)
- MGSF = TSOP−6, SOT−23

Current

Tape/Reel Designator

Optional Suffix
- E = Energy Rated
- HD = High Cell Density
- L = Logic Level
- V = TMOS V™ (Five)
- Z = ESD

Voltage Rating (Divided by 10)

Channel Polarity
- N or P
- C = Complementary

PREVIOUS FORMAT 2

M T P 75 N 06 HD

Circuit Identifier
- X = Engineering Samples

TMOS®
- T = TMOS
- L = SMARTDISCRETES™
- G = IGBT (Except MGSF)

Package Type
- P = Plastic TO−220
- D = DPAK
- A = TO−220 Isolated
- W = TO−247
- B = D2PAK
- Y = TO−264

Optional Suffix
- L = Logic Level
- E = Energy Rated
- T4 = Tape & Reel (DPAK/D2PAK)
- RL = Tape & Reel (DPAK)
- HD = High Cell Density
- V = TMOS V™ (Five)

Voltage Rating (Divided by 10)

Channel Polarity
- N or P

Current

PREVIOUS FORMAT 3

M M SF 4 2 05

Circuit Identifier

TMOS®
- M = Miniature

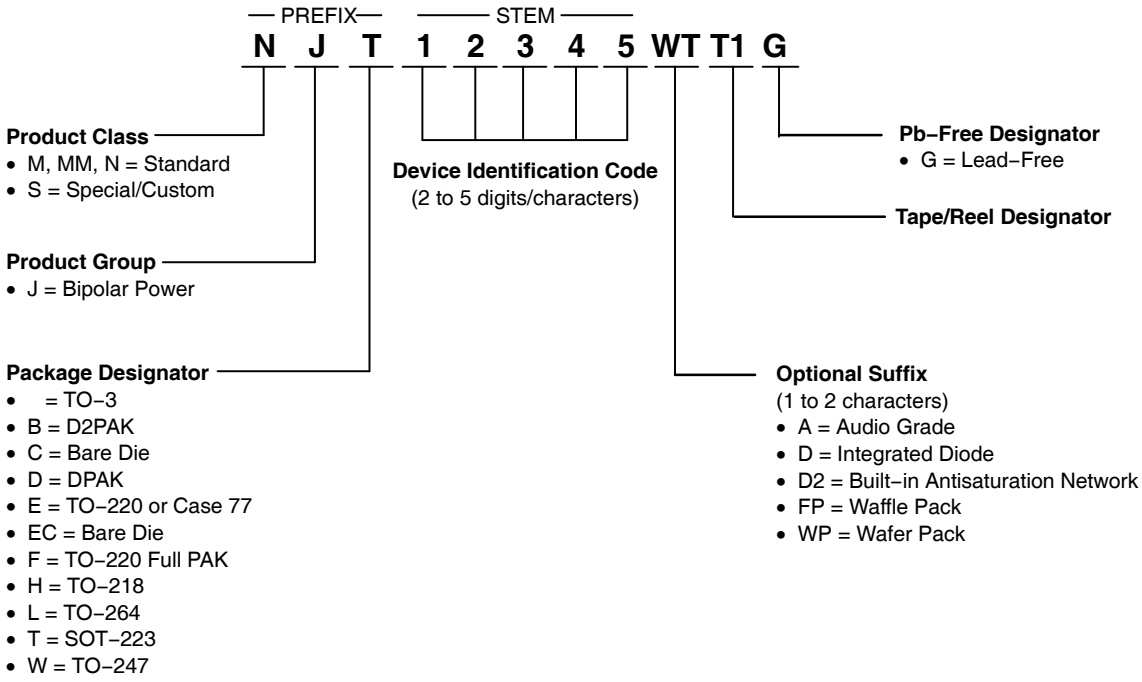
Package Type
- DF = Dual FET (SO−8)
- SF = Single FET (SO−8)
- FT = FET Transistor (SOT−223)
- MTSF = Single FET (Micro8)
- MTDF = Dual FET (Micro8)
- MGSF = TSOP−6, SOT−23

Technology
- 5 = Trench
- 4 = HD3e
- 3 = HD3
- 1 = HD1

Voltage + 10

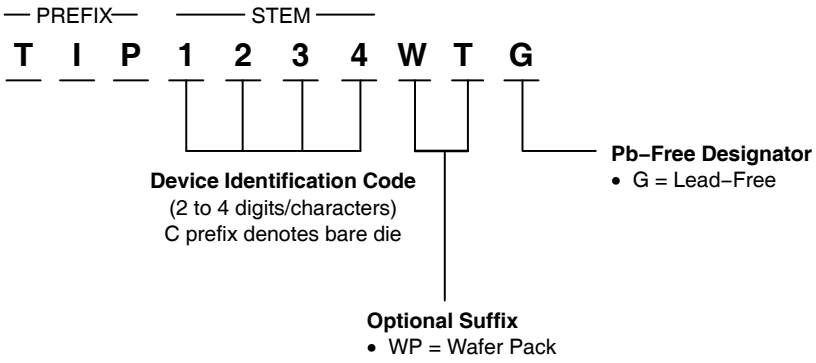
Even = N Channel
Odd = P Channel

Naming Convention for Bipolar Power Devices

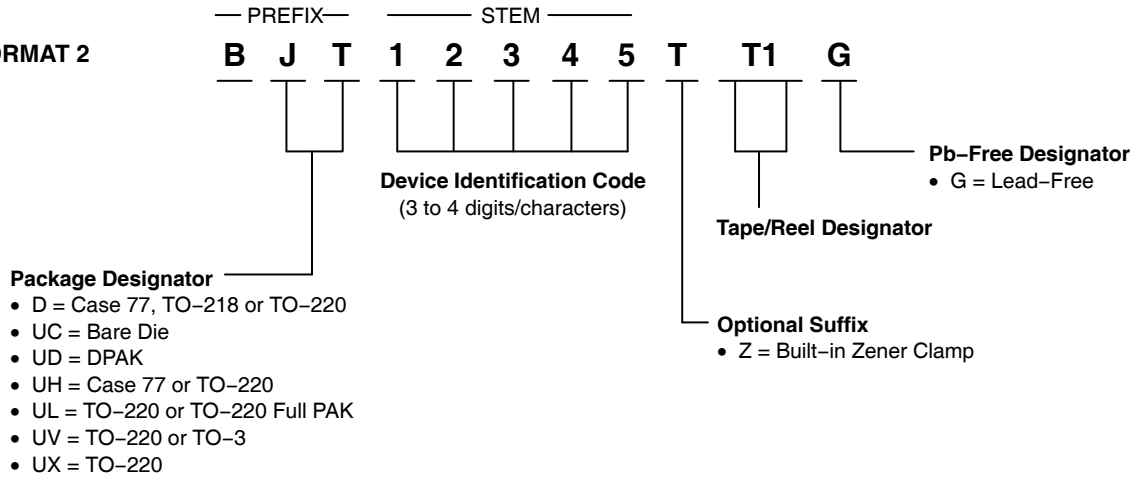


Naming Convention for Bipolar Power Devices

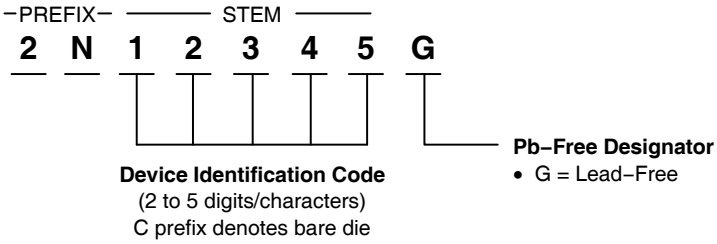
PREVIOUS FORMAT 1



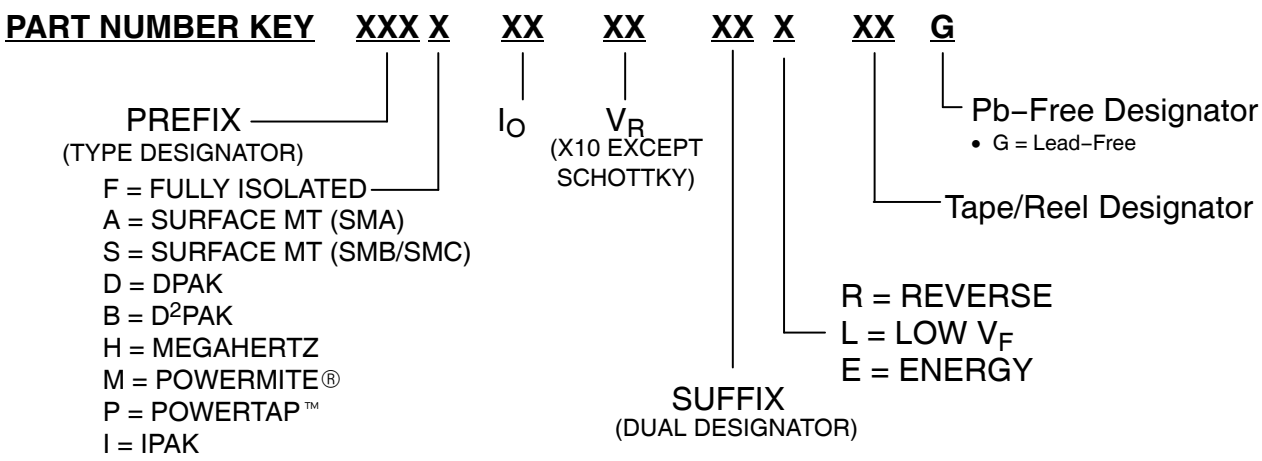
PREVIOUS FORMAT 2



PREVIOUS FORMAT 3



Naming Convention for Rectifier Devices



PREFIX KEY

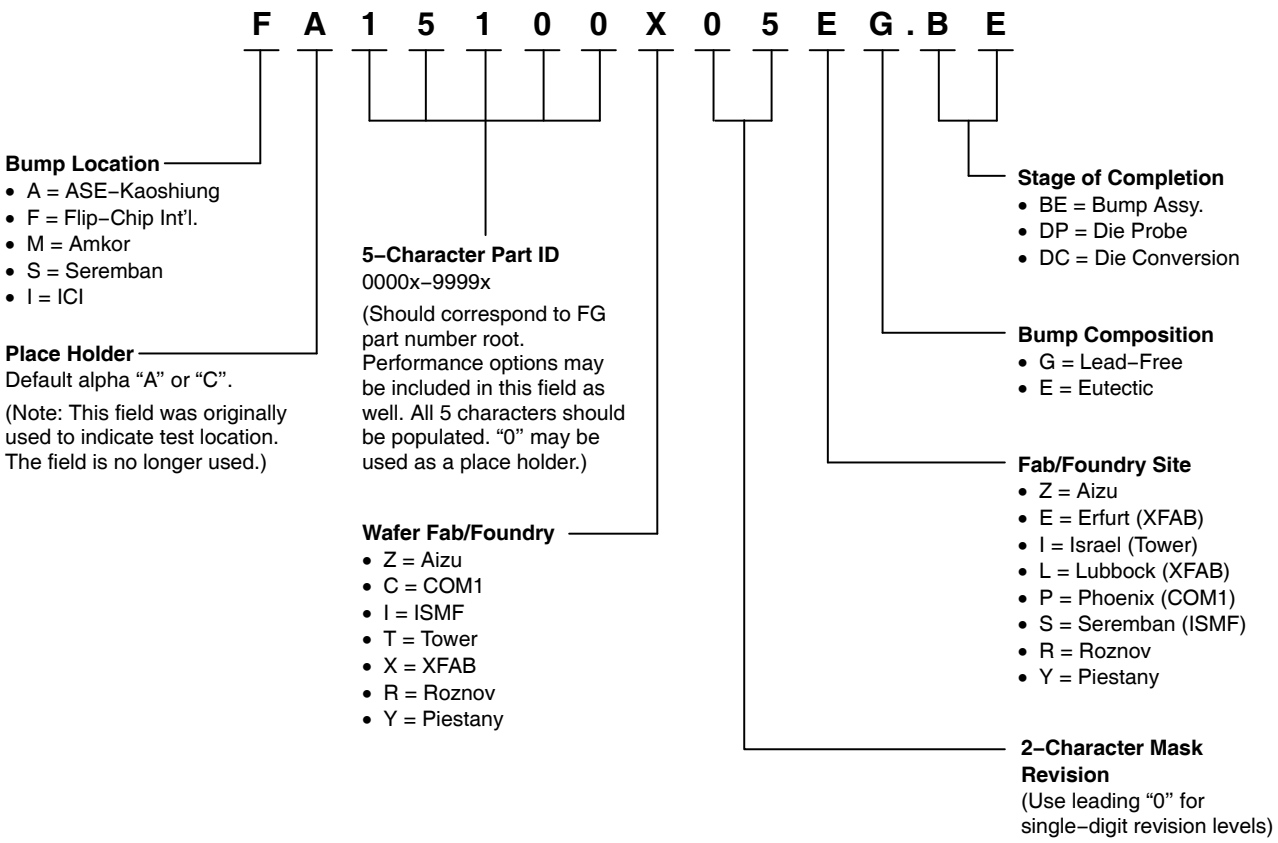
MUR = ULTRA FAST RECTIFIER
MBR = (SCHOTTKY) BARRIER RECTIFIER
MR = STANDARD & FAST RECOVERY
MSR = ULTRASOFT

SUFFIX KEY

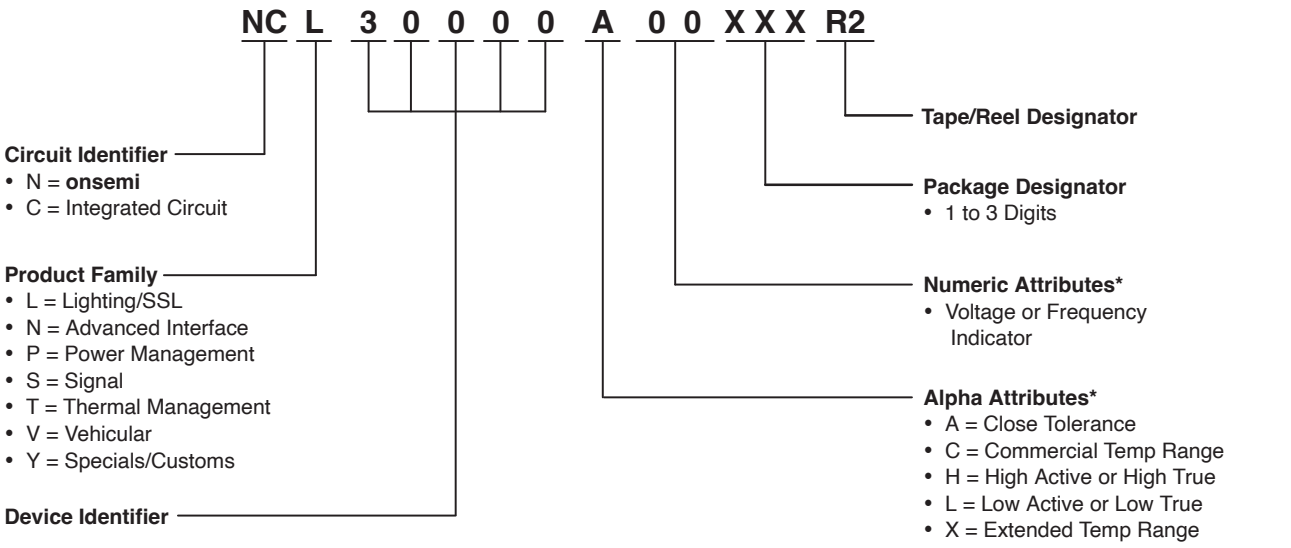
CT = CENTER TAP (DUAL) TO−220, POWERTAP, DPAK, D^{2}PAK
PT = CENTER TAP (DUAL) TO−218 PACKAGE
WT = CENTER TAP (DUAL) TO−247
SF = SOD−123 FLAT LEAD
PF = POWER FACTOR CORRECTION SPECIFIC

EXAMPLE:	MUR	30	20	WT
	ULTRAFAST	30 AMP	200 V	CENTER TAP (DUAL) TO−247
EXAMPLE:	MBR	30	45	WT
	SCHOTTKY	30 AMP	45 V	CENTER TAP (DUAL) TO−247

Naming Convention for FMO Bump



Naming Convention for LED/Lighting Products



* Optional

Naming Convention for Current Serial EEPROMs

N V 24C XXX M01 -1 X XXX TC G

Circuit Identifier
- N = Standard **onsemi**
- S = Customer Special

Product Class
- Blank = Industrial/Commercial
- V = Automotive

Product Interface

Current Generation
- 21 = 1-Wire
- 24C = I2C/SMB
- 25 = SPI
- 26 = I2C/SMB/SPI Combo
- 28 = I3C
- 29 = Microwire

Next Generation
- 31 = 1-Wire
- 34C = I2C/SMB
- 35 = SPI
- 36 = I2C/SMB/SPI Combo
- 38 = I3C
- 39 = Microwire

Product Family
- Blank = EEPROM
- RF = RF/NFC
- RFE = RF/NFC with Energy Harvesting
- TS = Temperature Sensor
- DP = Digital Potentiometer

EEPROM Memory Density
- 001 = 1 kb
- 002 = 2 kb
- 004 = 4 kb
- 008 = 8 kb
- 016 = 16 kb
- 032 = 32 kb
- 064 = 64 kb
- 128 = 128 kb
- 256 = 256 kb
- 512 = 512 kb
- M01 = 1024 kb
- M02 = 2048 kb

OR

Function Number (EEP+ and others)

Temperature Range
- -3 = -40 to +85°C
- -2 = -40 to +105°C
- -1 = -40 to +125°C
- -0 = -40 to +150°C
- -9 = Wide Temp Range

Special Option

A ... Z ** =
- Software Write Protect
- ID Page
- Low Voltage
- Different Slave Address
- Different Pinout
- Package Height
- Other Features

** Do not use the same character as the first character of the package code

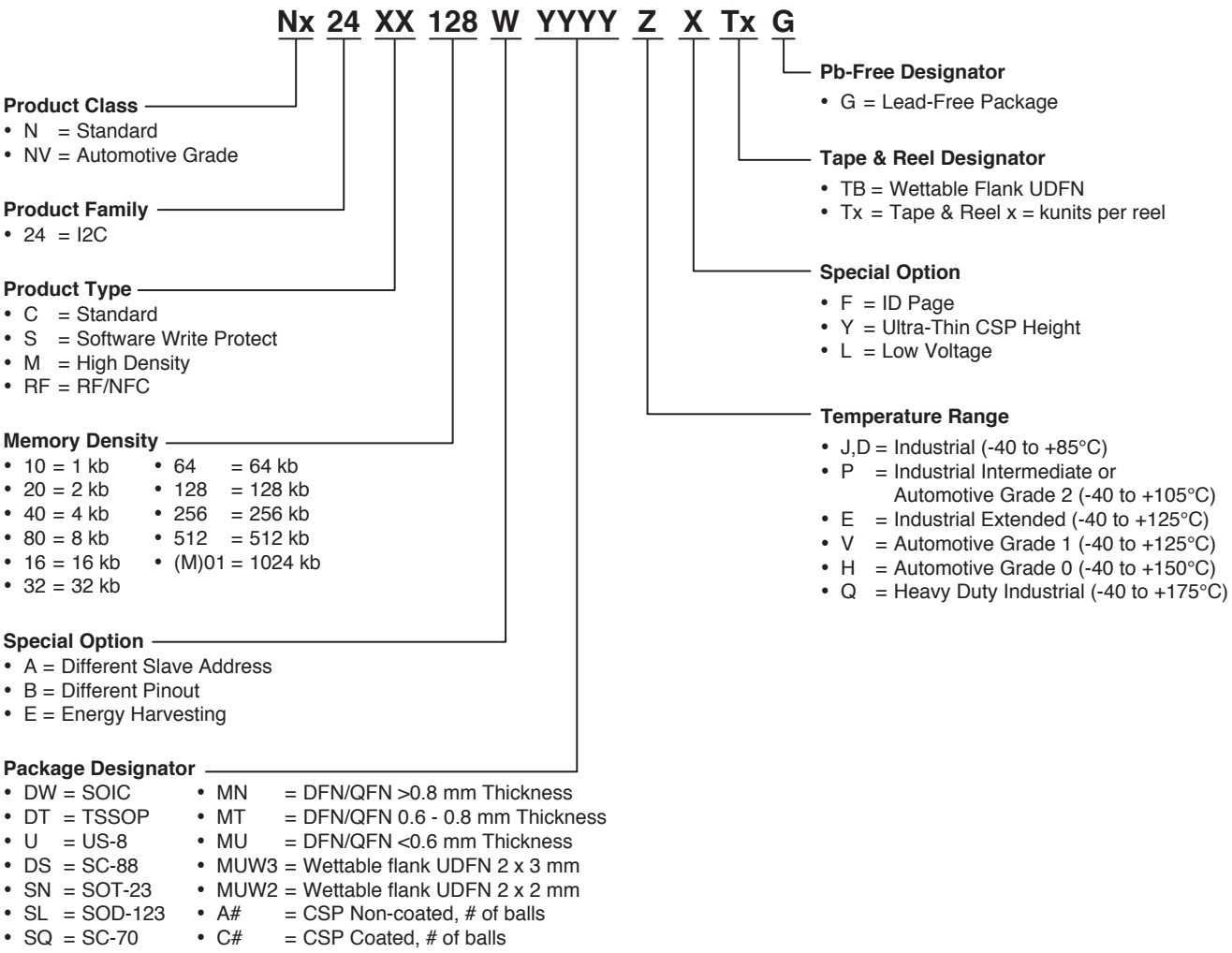
Package Options
- D = SOIC-NB
- DW = SOIC-WB
- DT = TSSOP
- US = US-8
- DF = SC-88/SC-70
- DT = SOT-23
- DBV = SC-74
- C = CSP Non-Back Coated
- CB = CSP Back Coated
- MNp* = DFN/QFN >0.8 mm Thickness
- MTp* = DFN/QFN 0.6 - 0.8 mm Thickness
- MUp* = DFN/QFN <0.6 mm Thickness
- MUp*W3 = Wettable Flank 2 mm Width
- MUp*W2 = Wettable Flank 3 mm Width

* p = Pin Pitch
- 1 = 0.05 mm
- 2 = 0.40 mm
- 3 = 0.35 mm

Tape & Reel Designator
- C = Tape & Reel Size/Pin 1 Orientation for Leadless Packages
- = See BRD8011/D for Other Packages

Pb-Free Designator
- G = Lead-Free Package

Naming Convention for I2C Serial EEPROMs



Naming Convention for SPI Serial EEPROMs

Nx 25 128 XXXX Y Z Tx G

Product Class
- N = Standard
- NV = Automotive Grade

Product Family
- 25 = SPI

Memory Density
- 010 = 1 kb
- 020 = 2 kb
- 040 = 4 kb
- 080 = 8 kb
- 160 = 16 kb
- 320 = 32 kb
- 640 = 64 kb
- 128 = 128 kb
- 256 = 256 kb
- 512 = 512 kb
- (M)01 = 1024 kb

Package Designator
- DW = SOIC
- DT = TSSOP
- MN# = DFN/QFN >0.8 mm Thickness
- MT# = DFN/QFN 0.6 - 0.8 mm Thickness
- MU# = DFN/QFN <0.6 mm Thickness
- MUW3 = Wettable flank UDFN 2 x 3 mm
- MUW2 = Wettable flank UDFN 2 x 2 mm
- U = US-8
- DS = SC-88
- SN = SOT-23
- SQ = SC-70
- A# = CSP Non-coated, # of balls
- C# = CSP Coated, # of balls

Temperature Range
- J,D = Industrial (-40 to +85°C)
- P = Industrial Intermediate or Automotive Grade 2 (-40 to +105°C)
- E = Industrial Extended (-40 to +125°C)
- V = Automotive Grade 1 (-40 to +125°C)
- H = Automotive Grade 0 (-40 to +150°C)
- Q = Heavy Duty Industrial (-40 to +175°C)

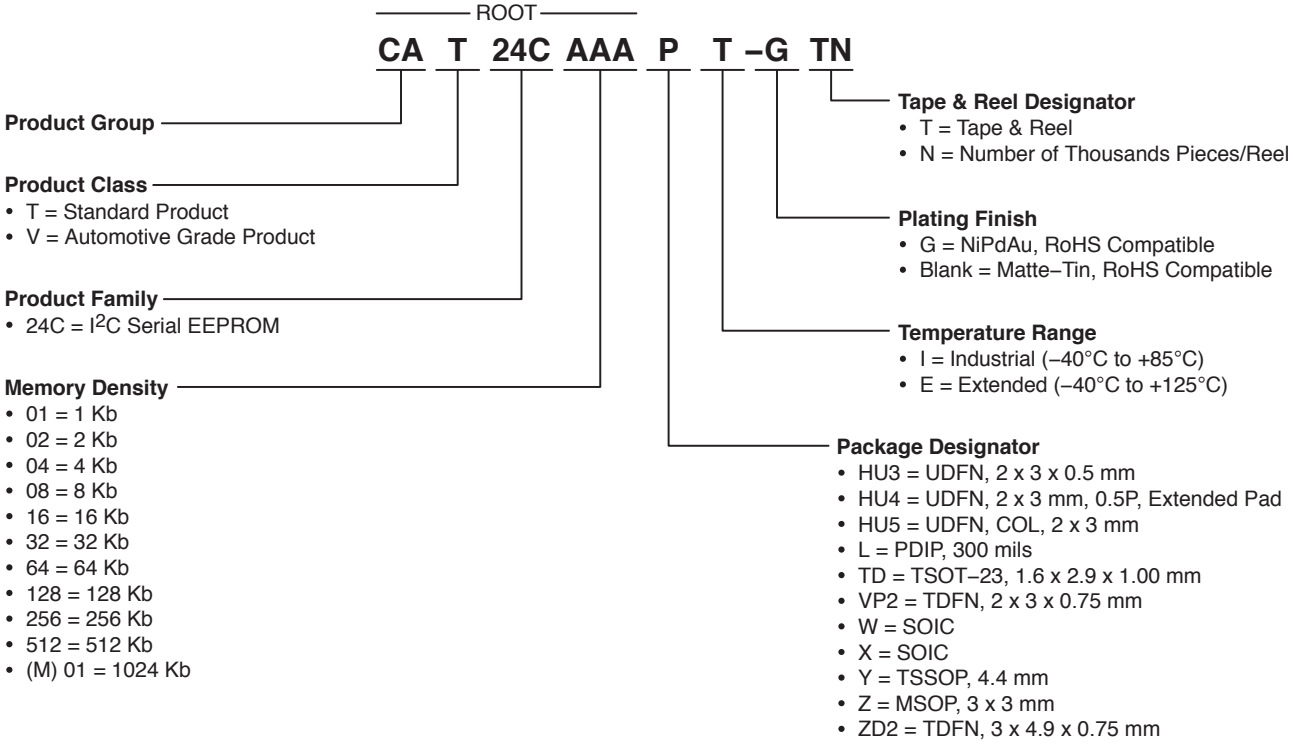
Special Option
- F = ID Page
- Y = Ultra-Thin CSP Height
- L = Low Voltage

Tape & Reel Designator
- TB = Wettable Flank UDFN
- Tx = Tape & Reel x = kunits per reel

Pb-Free Designator
- G = Lead-Free Package

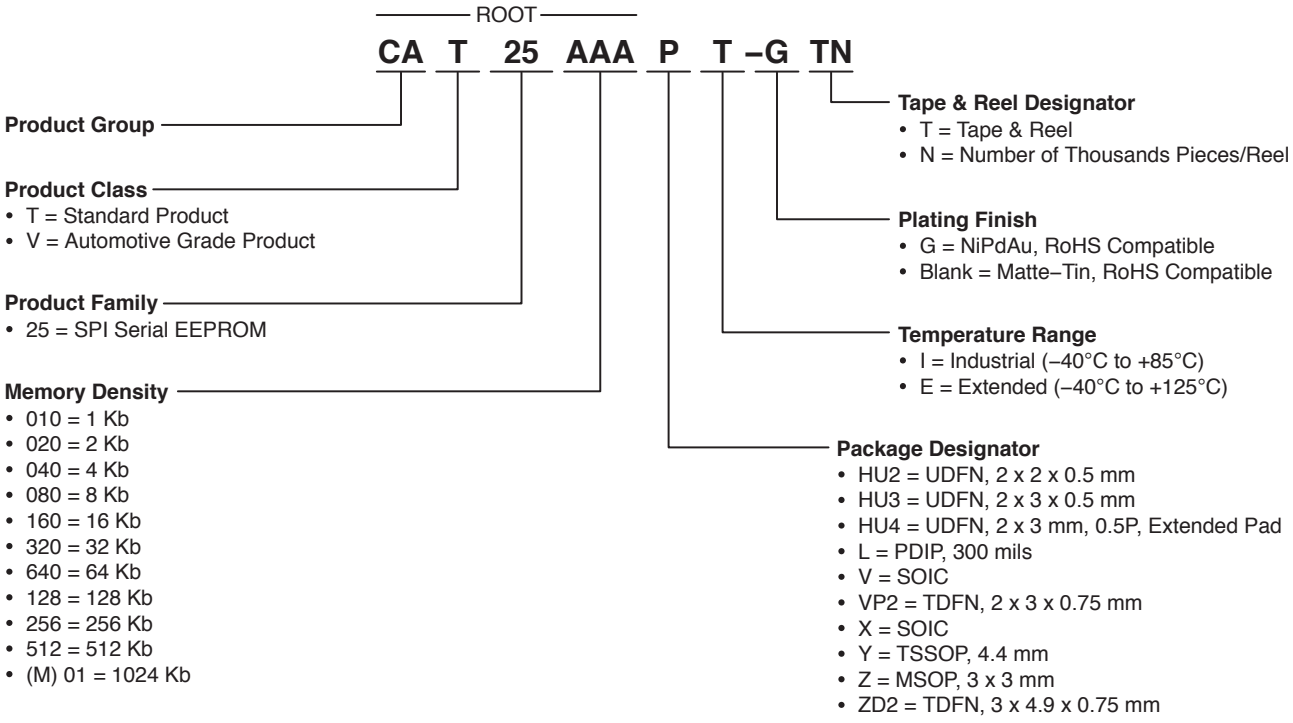
Naming Convention for Legacy I2C Serial EEPROMs

(Formerly Catalyst Semiconductor)



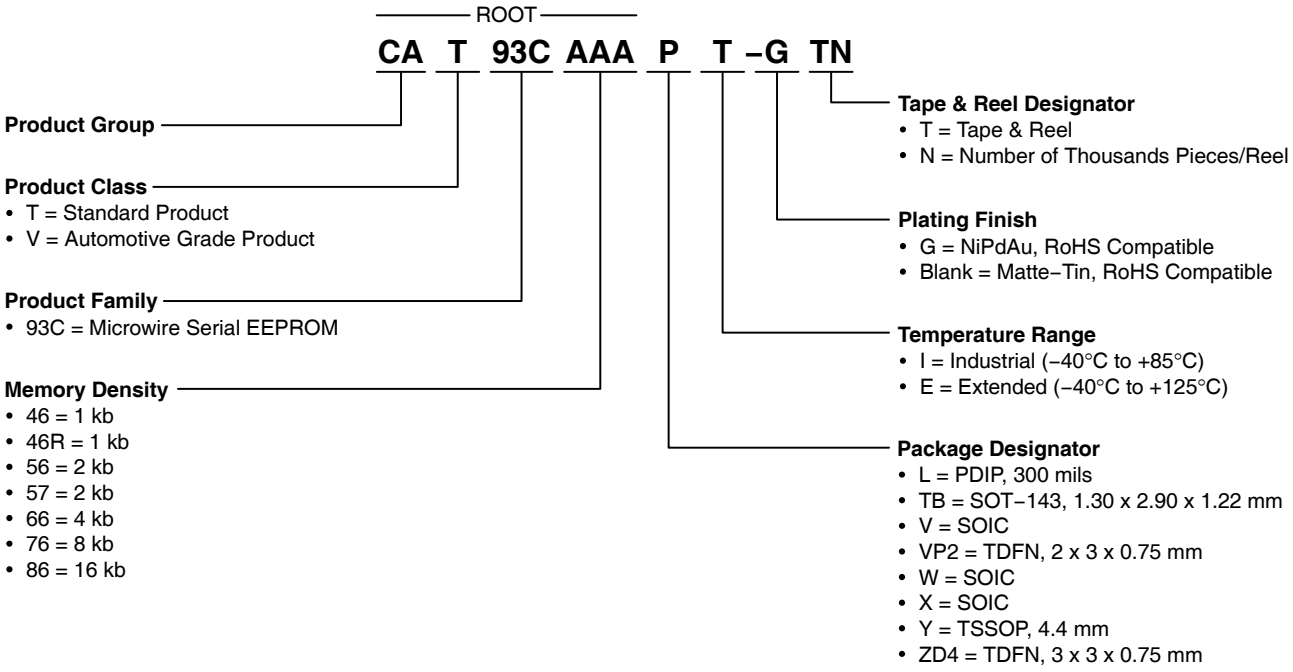
Naming Convention for Legacy SPI Serial EEPROMs

(Formerly Catalyst Semiconductor)

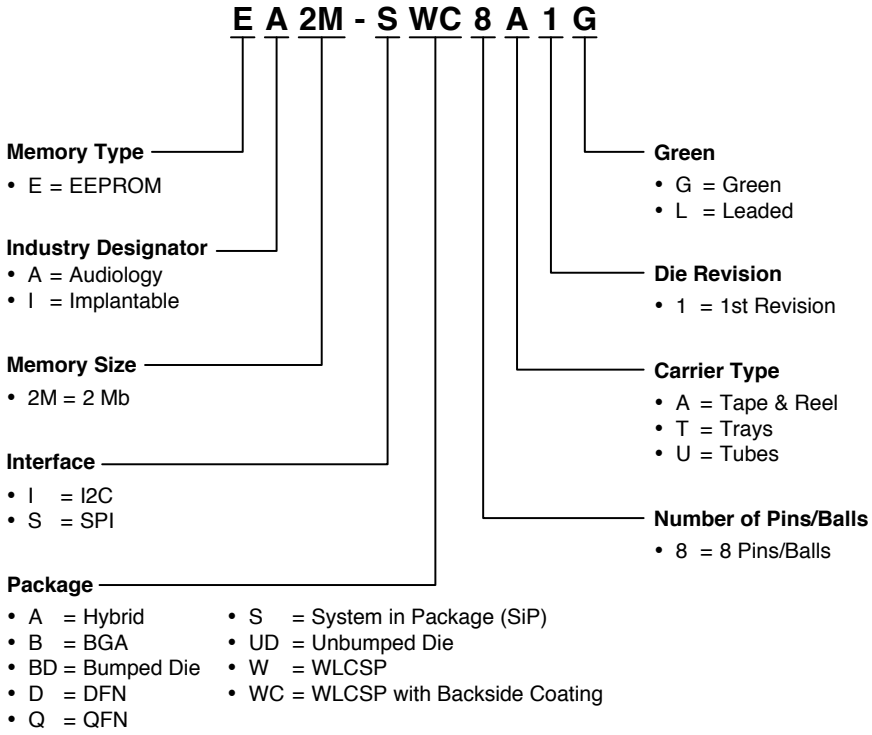


Naming Convention for Microwire Serial EEPROMs

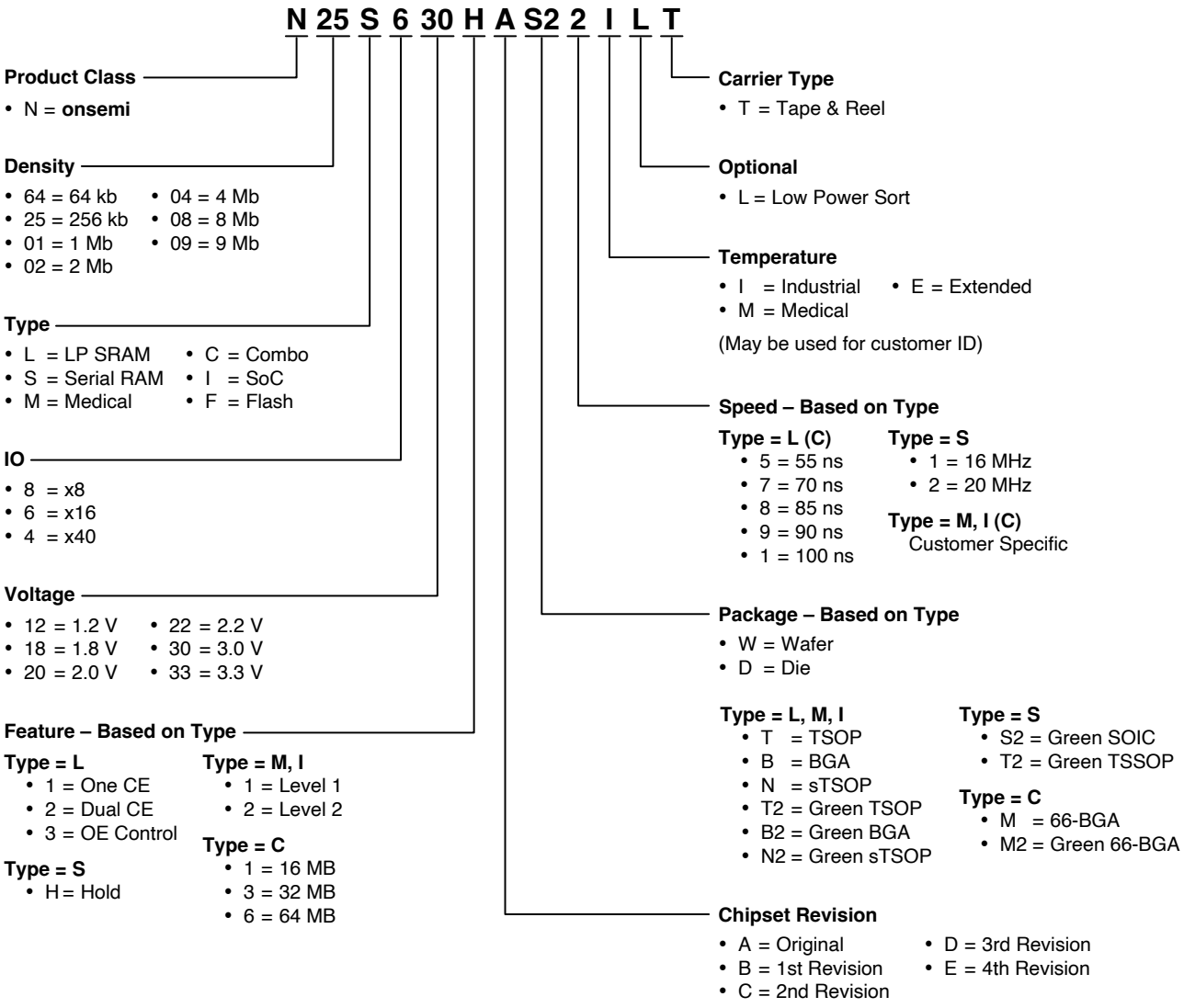
(Formerly Catalyst Semiconductor)



Naming Convention for EEPROM Memory

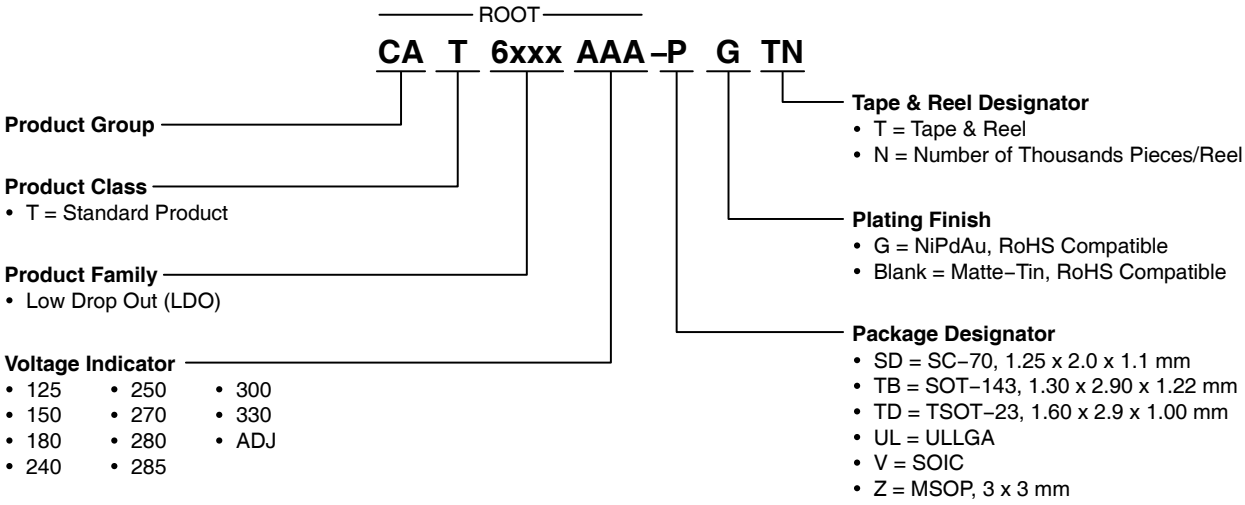


Naming Convention for Memory Products



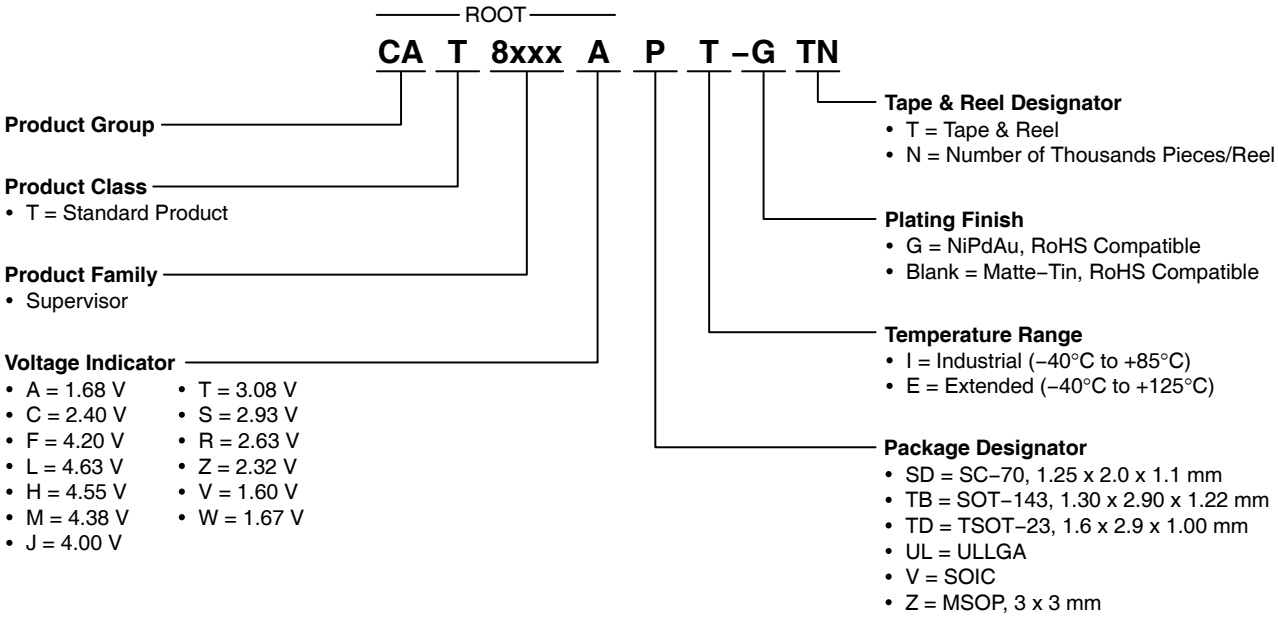
Naming Convention for Low Drop Out (LDO) Products

(Formerly Catalyst Semiconductor)



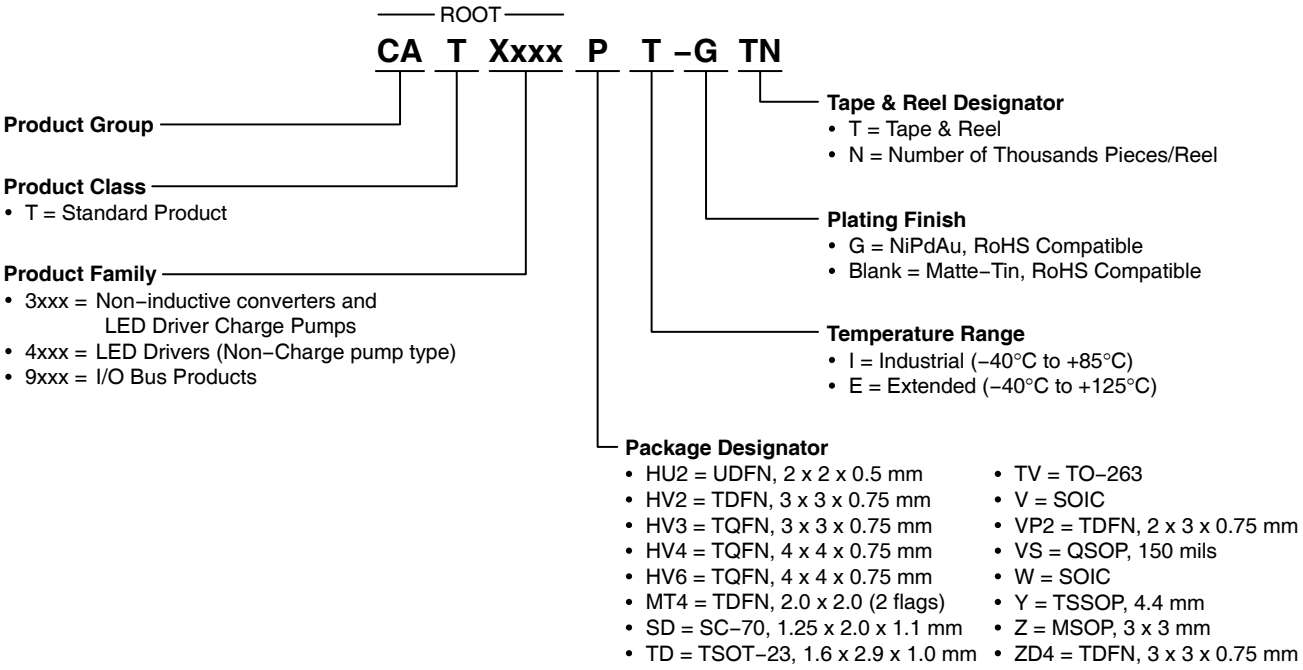
Naming Convention for Supervisor Products

(Formerly Catalyst Semiconductor)



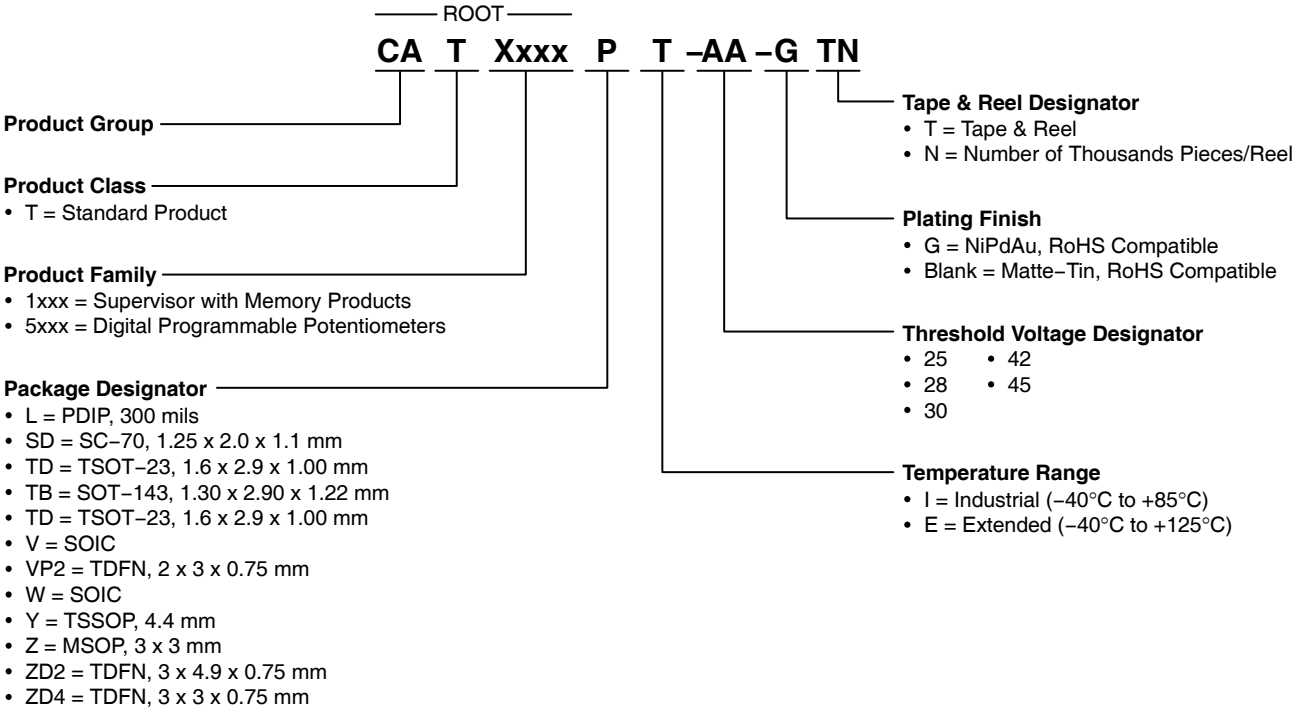
Naming Convention for Charge Pumps, LED Drivers, and I/O Bus Products

(Formerly Catalyst Semiconductor)



Naming Convention for Digital Programmable Potentiometers and Supervisor with Memory Products

(Formerly Catalyst Semiconductor)



Naming Convention and Ordering Information for ASIC Devices

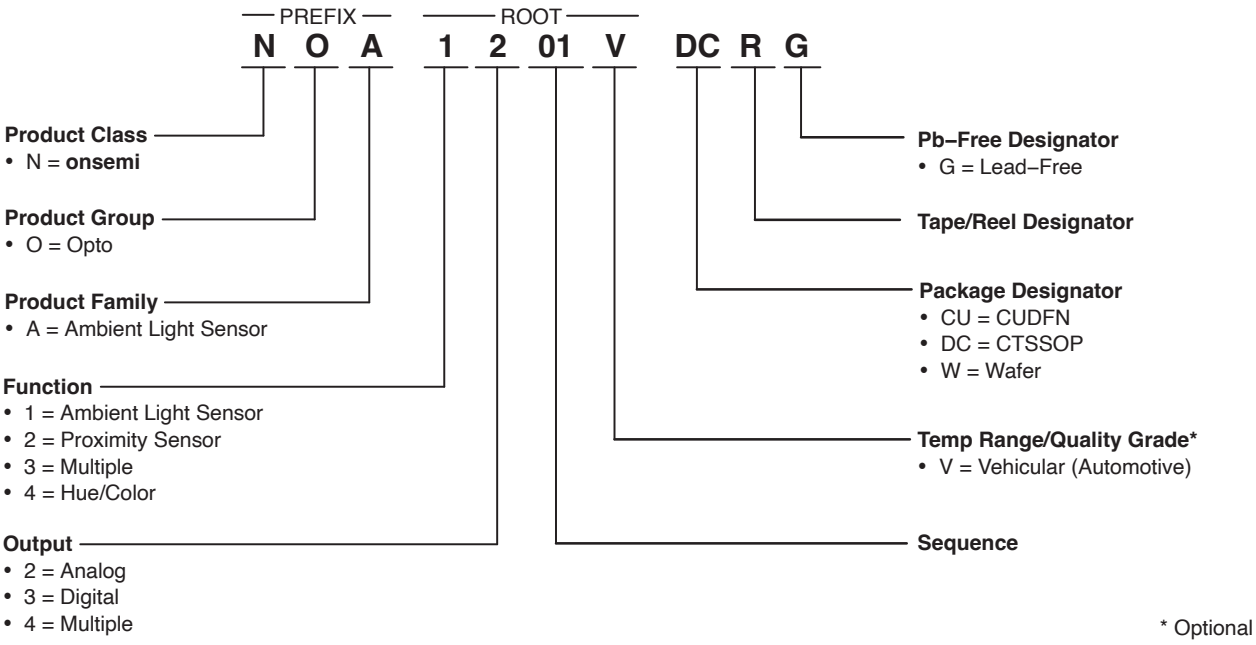
12345–123 – ABC

Device Number
5–3 Digit Alpha–Numeric

Packing Form Designator
- XWF = Wafer Form
- XSW = Sorted Wafer
- XDW = Die in Wafer Form
- XDI = Die
- XDF = Die in File Frame
- XDS = Die in Tape
- XUD = Untested and Packaged
- XUP = Untested and Packaged in Tape & Reel
- XTD = Tested and Packaged in Trays or Tubes
- XTP = Tested and Packaged in Tape & Reel
- XPD = Photo Diode Array
- XMD = Module

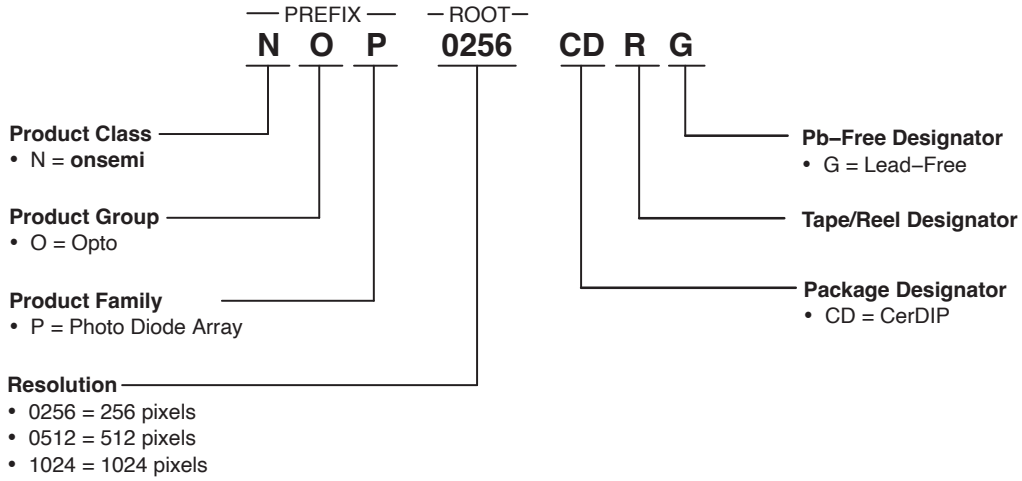
Notes:
1. Not all packing forms are available for each product.
2. Contact **onsemi** Customer Service for more details.

Naming Convention for Ambient Light Sensor Devices

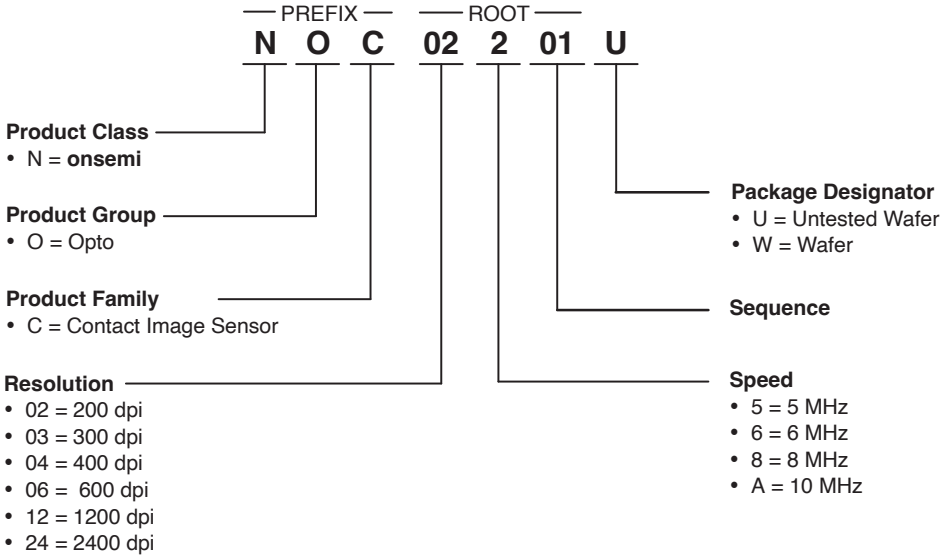


* Optional

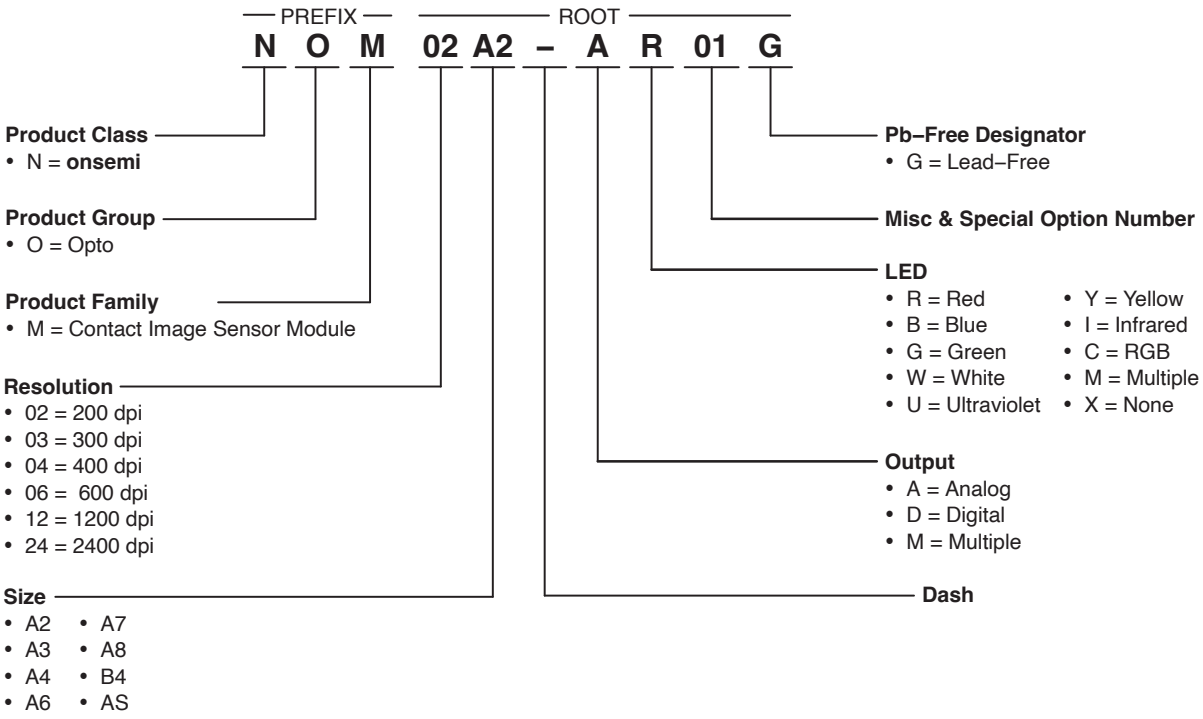
Naming Convention for Photo Diode Array Devices



Naming Convention for Contact Image Sensor Devices

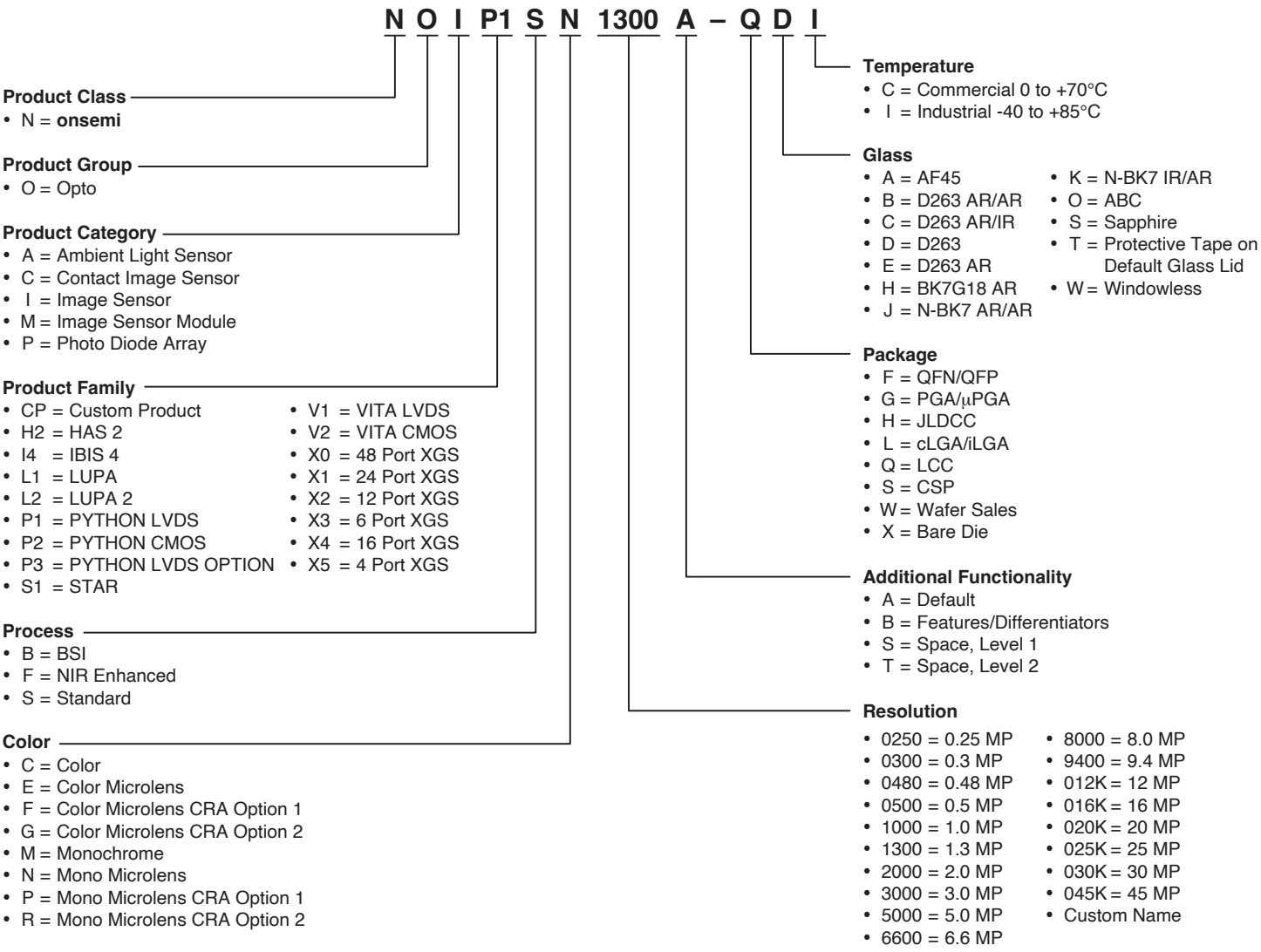


Naming Convention for Contact Image Sensor Modules



Naming Convention for Image Sensors

(Formerly Cypress Semiconductor)



Naming Convention for Image Sensors

(Formerly Truesense Imaging, Inc.)

K AI - 290 50 - CXA - DD - AA

Product Line
- K = Image Sensors

Family Designation
- AF = Full Frame CCD
- AI = Interline CCD
- AE = Interline EMCCD
- LI = Linear CCD
- SC = Support Chip
- AC = CMOS
- AT = TDI CCD

Resolution (2 or 3 Digits)

Specified in units of 100 K pixels,
e.g. 290 = 29.0 Mega Pixels

Sequence (2 Digits)

Color Filter Array
- A = No CFA (Monochrome)
- B = Pigment, Bayer CMY
- C = Pigment, Bayer RGB
- D = Pigment, Linear RGB
- E = 3G Stagger
- F = Pigment, Bayer RGB, Gen 2
- G = Striped RGRB
- H = RB Checkerboard
- J = Hybrid Dichroic
- L = RBG and Mono
- M = Mono with RB Surround
- N = Pigment, Bayer RGB, Shorter Red Wavelength
- P = Sparse CFA Pattern A
- Q = Sparse CFA Pattern A, Gen 2
- R = Pigment, Linear RGB, Gen2
- S = Mono with RB Surround, Gen2
- X = Special

Microlens
- A = No microlenses
- B = Telecentric microlenses
- C = Cylindrical microlenses
- D = None with spacer (Not for UV or bundle attachment)
- E = Telecentric, microlenses, enhanced ultraviolet
- X = Special

Product Revision

Package
- A = Wafer Form (No Pkg)
- B = Die Form (No Pkg)
- C = Cerdip, Sidebrazed Pins
- D = Cerdip, Sidebrazed Pins, CuW
- E = Cerdip, Leadframe
- F = CLCC
- G = PLCC
- H = Plastic DIP
- J = PGA
- K = PGA, CuW Base
- L = QFP
- M = CSP
- N = Bare Die, Reconstituted Wafer
- P = Polyimide Substrate
- Q = Aluminum Nitride Substrate
- R = pLLP
- S = PGA, CuW Base, TEC Cooler
- X = Special

Cover Glass
- A = No Glass
- B = Clear, No Coatings
- C = Clear, AR Coated 1 Side
- D = Clear, AR Coated 2 Sides
- E = Clear, AR Coated Side 1, IR Coated Side 2
- F = Quartz, No Coatings
- G = Plastic, No Coatings
- H = IR Absorbing, AR Coated 2 Sides
- J = Clear, AR Coated 2 Sides, with Light Shield
- K = Quartz, AR Coated 2 Sides
- L = Hermetic, AR Coated 2 Sides
- P = Clear, No Coatings (Taped)
- Q = Clear, AR Coated 1 Side (Taped)
- R = Clear, AR Coated 2 Sides (Taped)
- S = Quartz, No Coatings (Taped)
- X = Special

Testing Method
- A = Standard
- B = Standard with Defect Map
- C = Non-Standard
- D = Non-Standard with Defect Map
- E = Low Temperature
- F = Low Temperature with Defect Map
- G = Customer Specific
- H = Standard with Special Visual
- X = Special

Product Grade
- 0 = Highest Grade (Fewest Cosmetic Defects)
- 1 = Cosmetic Specs Relaxed Relative to Grade 0
- 2 = Cosmetic Specs Relaxed Relative to Grade 1
- 3 = Cosmetic Specs Relaxed Relative to Grade 2
- A = Standard Grade: Used when only one grade is available for a given product.
- C = Commercial Grade: Meets all specification criteria, but have not been fully qualified. Intended for evaluation purposes only and have NO warranty. Quantities are strictly limited and sold only “as available”.
- E = Engineering Grade: Electrically functional and meet most, but not necessarily all, product performance specifications, however there are no limitations on the number of or size of cosmetic defects (points, clusters, columns, glass defects, etc.) allowed. Intended for evaluation purposes only and have NO warranty. Quantities are strictly limited and sold only “as available”.
- T = Test Sample: Closely resembles the performance of the final product, however may not meet any of the specification criteria. Intended for evaluation purposes only and have NO warranty. Quantities are strictly limited and sold only “as available”.
- M = Mechanical Sample: Meets all physical dimensions and tolerances and likely does not image. Intended for evaluation purposes only and have NO warranty. Quantities are strictly limited and sold only “as available”.
- X = Special

Naming Convention for Image Sensors

(Formerly Aptina Imaging Corporation)

Base Part Number

A S 05 4 0 HD 8 C 22 S H D2 0 - XX - YYYYY - E

Product Line
- A = Image Sensors

Product Type
- S = SOC
- R = RAW Sensor
- P = ISP
- F = iToF
- G = Generic
- B = Bridge
- D = Downgrade

Resolution
- Y1 = 0.01 Megapixel
- Y2 = 0.02 Megapixel
- Y9 = 0.09 Megapixel
- X1 = 0.1 Megapixel
- X9 = 0.9 Megapixel
- 01 = 1 Megapixel
- 99 = 99 Megapixel
- B1 = Demo3 Base Board
- B2 = Demo3 Adapter - Old Style HB
- B3 = Demo2x Adapter - New Style HB
- B4 = ICP Adapter Board
- B5 = Stereo Receiver Board
- A1 = 100-199 M
- A2 = 200-299 M
- A3 = 300-399 M
- NN = N/A

Optical Format
- 0 = >1" or ISP
- 1 = 1"-2"
- 2 = 1/2"
- 3 = 1/3"
- 4 = 1/4"
- 5 = 1/5"
- 6 = 1/6"
- 7 = 1/7"
- 8 = 1/8"
- 9 = 1/9"
- A = 1/10"
- B = 1/11"
- C = 1/12"
- D = 1/13"
- G = 2/3"
- H = APS-H/35 mm
- I = 2"-3"
- J = 3"-4"
- K = 4"-5"
- N = N/A

Unique Product Identifier (ID)

Must increment for a new product with the same resolution and optical format (e.g., each new ¼" VGA part increments this by one). Sequence 0, 1, 2…9, A, B,…Z .

Marketing Descriptor

Provides marketing ability to add additional descriptive information that may be helpful in positioning the part.
- CS = Default, CMOS Sensor
- PD = Phase Detection
- IR = Infrared
- NP = NIR (CSD)
- HS = High Speed
- SR = Surveillance
- MD = Medical
- CM = Camera
- AT = Automotive

Major "Imager Customer" Revision

Revision number 1~9 shown during development and initial release
Revision "S" will replace number after full production release
for long-running products

Chromaticity
- C = RGB
- M = Monochrome
- Y = CMY
- R = RCCC
- G = RGBC
- B = RCCB
- S = Common
- L = Logic
- A = Color Array
- N = Mono Array
- E = RCCG
- F = RYYB
- H = RGBIR
- P = RYYCy
- X = N/A

CRA Degree

"00" as N/A, otherwise will show
the actual degree shift

Sample and Demo Board Identifier
- E = Eng Identifier (AS/ES/QS)
- M = Mechanical Sample
- GEVB = Demo Board
- GEVK = Demo Kit
- Blank = Production Part

Mechanical Finish, Glass, Wafer Thickness*

See definitions on following page

Customer Special

Customer specific attribute

Special Options
- 0 = Default, N/A
- D = Demo Board
- H = Head Board
- S = High Speed
- D3 = Demo Kit (Demo3)
- Q = Adapter/FBGA/ASIC Board
- R = Reference Board
- H3 = Demo Headboard
- X = NIR (ASD)
- 1-9 = Other Special Variant

Package Options
- A = Lead Free
- B = Leaded
- C = Halogen Free
- D = 7.5 x 7.5 Lead Free
- E = 9.5 x 9.5 Lead Free
- F = 5.5 x 5.5 Lead Free
- M = MCP (Stack Packaging)
- Z = BIB/HIB Option (Different Bond Option)
- 0 = Module
- 1 = 100 μm Thickness
- 2 = 200 μm Thickness
- 3 = 305 μm Thickness
- 4 = 400 μm Thickness
- 6 = 675 μm Thickness
- 9 = No-Grinding

Package Type
- A = CLCC
- B = PLCC
- C = ILCC
- D = Die Sales
- E = IBGA
- F = LBGA
- G = VFBGA
- H = CPGA
- J = TPLCC
- K = CSP
- L = WLC
- M = CLGA
- N = imBGA
- P = tpBGA
- Q = iCBGA
- R = mPLCC
- S = IEBGA
- T = mPBGA
- U = ILGA
- W = Wafer Sales (EA)
- Y = Wafer Sales (WFR)

Interface Type
- M = MIPI
- C = CCP/CCP2
- H = HISPI
- U = MULTI
- E = Ethernet
- N = N/A
- P = PARALLEL
- L = LVDS
- S = SLVS

Operating Temp
- S = Commercial
- A = Automotive (–40 to +85°C)
- X = Extended (–40 to +105°C)
- N = N/A

Naming Convention for Image Sensors

(Formerly Aptina Imaging Corporation)

Packaged Parts

- D P BR 1

Mechanical Finish
- D = Dry Pack
- T = Tape & Reel
- C = Chiptray

Protective Film
- P = With Protective Film
- R = Without Protective Film

MPQ Option

Used only when there at two MPQ options for same part
- Empty = Default
- 1 = Single Tray
- RC1 = Fixed Number of Film Frames (Recon)

Glass Type
- Blank = Standard Glass
- BR = Double Side AR Glass
- AR = Single Side AR Glass
- IR = Single Side IR Glass
- IA = Infrared Cut-Off Filter/IRFC
- AM = Single Side AR Glass with Mask
- BM = Double Side AR Glass with Mask

Wafer and Die Sales

- 200

Wafer Thickness
- 200 = Wafer Thickness

Demo Board Special

- S213A

Mechanical Finish
- S213A = DSL213A
- S115 = SUNEX_DSL115

Naming Convention for Image Sensor Adapter Boards

(Formerly Aptina Imaging Corporation)

A G B1 N 0 CS - XXXX

Product Line

onsemi formerly Aptina

Product Type
- S = SOC
- R = RAW Sensor
- P = ISP
- T = Test Chip
- D = Downgrade
- G = Generic

Board Type
- B1 = Demo3 Base Board
- B2 = Demo3 Adapter - Old Style HB
- B3 = Demo2x Adapter - New Style HB
- B4 = ICP Adapter Board
- B5 = Stereo Receiver Board
- B6 = AP21029 Generic Adapter
- B7 = AP1300 ICP2 Adapter
- B8 = AP21023 Beagle Board
- B9 = AP21070 Arndale Adapter
- BA = Series
- BB = Radar Series
- BC = X-CUBE
- BD = AP21109 Power Measurement

Optical Format
- 0 = >1” or ISP
- 1 = 1”
- 2 = 1/2”
- 3 = 1/3”
- 4 = 1/4”
- 5 = 1/5”
- 6 = 1/6”
- 7 = 1/7”
- 8 = 1/8”
- 9 = 1/9”
- A = 1/10”
- B = 1/11”
- C = 1/12”
- D = 1/13”
- N = N/A”

Sample and Demo Board Identifier
- GEVB = SOC
- GEVK = RAW Sensor

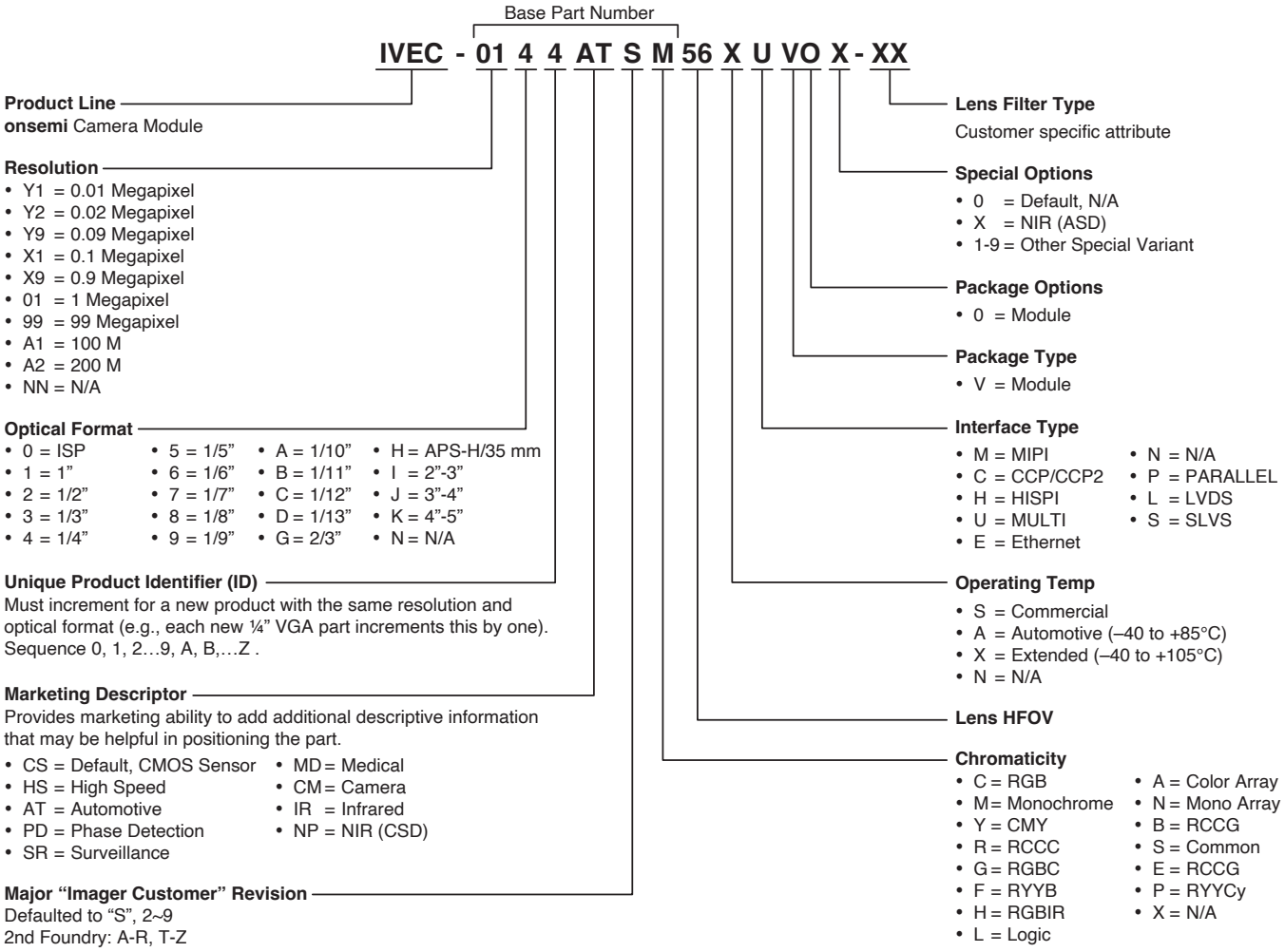
Marketing Descriptor

Provides marketing ability to add additional descriptive information that may be helpful in positioning the part.
- CS = Default, CMOS Sensor
- HS = High Speed
- AT = Automotive
- PD = Phase Detection
- SR = Surveillance
- MD = Medical
- CM = Camera
- IR = Infrared
- NP = NIR (CSD)

Unique Product Identifier (ID)

Must increment for a new product with the same resolution and optical format (e.g., each new ¼” VGA part increments this by one). Sequence 0, 1, 2…9, A, B,…Z .
- 2 = AP21057 Demo3 to AS0260 BYD Adapter
- 3 = AP21098 Demo3 to MT9M114 BYD Adapter
- 4 = AP21099 Demo3 to AR0833BYD Adapter
- 5 = AP22030 Ethernet Adapter
- 6 = AP21088 Frame Buffer Board
- 7 = AP40019 LFM Test Board
- 8 = AP21057 AP1300 HB to Dual HB Adapter
- 9 = AP21096 Cameralink HB to Demo3 Adapter
- A = NR4401
- B = AP21121 X-Cube IAS-Demo3 Adapter Board
- C = AP21094 Demo3 HB to Cameralink Demo Board
- D = AP21109 Power Measurement Adapter Demo3 Board HB

Naming Convention for Camera Module



Naming Convention for Legacy Image Sensors

(Formerly Aptina Imaging Corporation)

MT9 J 0 0 1 I12 ST C V xxxxxx ES

Product Line
- MT9 = Image Sensors, Legacy

Product Size
- C = CIF
- V = VGA
- M = 1 Meg
- D = 2 Meg
- T = 3 Meg
- Q = 4 Meg
- P = 5 Meg
- E = 8 Meg
- N = 9 Meg
- J = 10 Meg
- W = 12 Meg
- F = 14 Meg
- H = 16 Meg
- S = Special/Custom

Product Type
- 0 = Sensor Only
- 1 = SOC
- 2 = "Open"
- 3 = DSP
- 4 = High Speed
- 5 = Custom
- 6 = Others

Product Group
- 0 = Consumer Camera
- 1 = Mobile/PC
- 2 = Automotive/Industrial
- 3 = Surveillance

Unique Product Identifier (ID)

Must increment for a new product with the same resolution and optical format (e.g., each new ¼" VGA part increments this by one). Sequence 0, 1, 2…9, A, B,…Z .

PACKAGE CODE

Material/Construction
- A = TSV-RDL
- C = Ceramic
- X = Xintec
- E = Tessera
- P = Plastic
- S = Shellcase
- I = Imager
- L = Laminate
- T = Tiny
- Z = CWL CSP
- M = WLC

Form

Form 1: Form
- D = Singulated Die
- W = Die in Wafer Form
- M = Module
- B = Demo Base Board
- R = Demo Received Board
- V = LVDS Adapter Board

Package Type
- 0 = CSP
- 1 = LCC Pb-Free
- 2 = ICSP
- 3 = PGA
- 4 = QFP
- 5 = Custom
- 6 = Bumped
- 7 = BGA
- 8 = CSP Pb-Free
- 9 = ICSP Pb-Free
- A = BGA Pb-Free
- B = MVP
- C = Non-Bumped TSV-RDL
- D = Low Profile

Form 2 = 0

Leads/Bumps/Pins
- 0 = 32
- 1 = 28
- 2 = 48
- 3 = 64
- 4 = 144
- 5 = 208
- 6 = 280
- 7 = 52
- 8 = 30
- 9 = 44
- A = 35
- B = 13
- C = 84
- D = 137/169
- E = 16
- F = 38
- G = 116
- H = 122
- J = 54
- K = 25
- L = 55
- M = 67
- N = 120

Form 3 = 0

Note: If using Form 1, Form 2 (Package Type) and Form 3 (Leads/Bumps/Pins) will be "0"

Special Processing
- AS = Alpha Sample
- ES = Engineering Sample
- MS = Mechanical Sample
- MC = Module Camera Demo System
- I = Errata
- :X = DID Mark Designator
- Blank = Mass Production

Design ID and Probe/Test Level

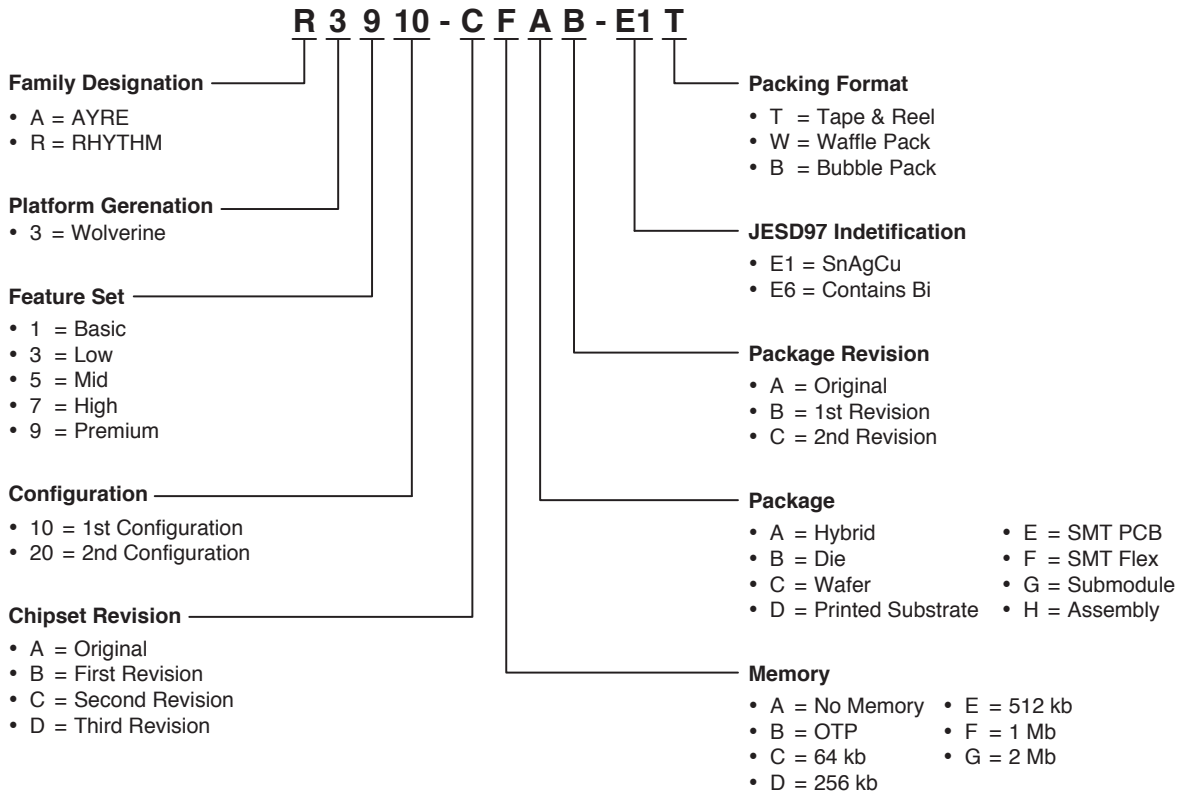
Six characters will appear for Die/ Wafer Only

Special Options
- A = Lens Head Board and Adapter Kit
- B = Non-Standard CRA
- C = Non-Standard CRA 27 Degrees
- D = Demo Board
- E = Recon (RDL)
- F = Frame Grabber
- G = WLM Socketed Headboard
- H = Head Board
- I = IR Glass
- J = JPEG Output
- K = Special Die Offset
- L = Lens Eval Kit
- M = MiPi
- N = No Lid
- P = CCP
- Q = Optical Quality
- LC = Low Cost
- R = Reference Camera
- S = High Speed
- T3 = Tier 3
- U = Parallel Interface
- V = Serial Interface
- W = NTUB
- X = No Micro Lens
- Y = Black Solder Mask
- Z = Non-Standard Micro Lens Shift
- PF = Protective Film
- 2 = 200 μm Wafer Thickness
- 3 = 305 μm Wafer Thickness
- 4 = 200 μm Thick Cover Glass
- 5 = 300 μm Thick Cover Glass
- 6 = 675 μm Wafer Thickness
- 7 = EMI Pad
- 8 = Non-Coating

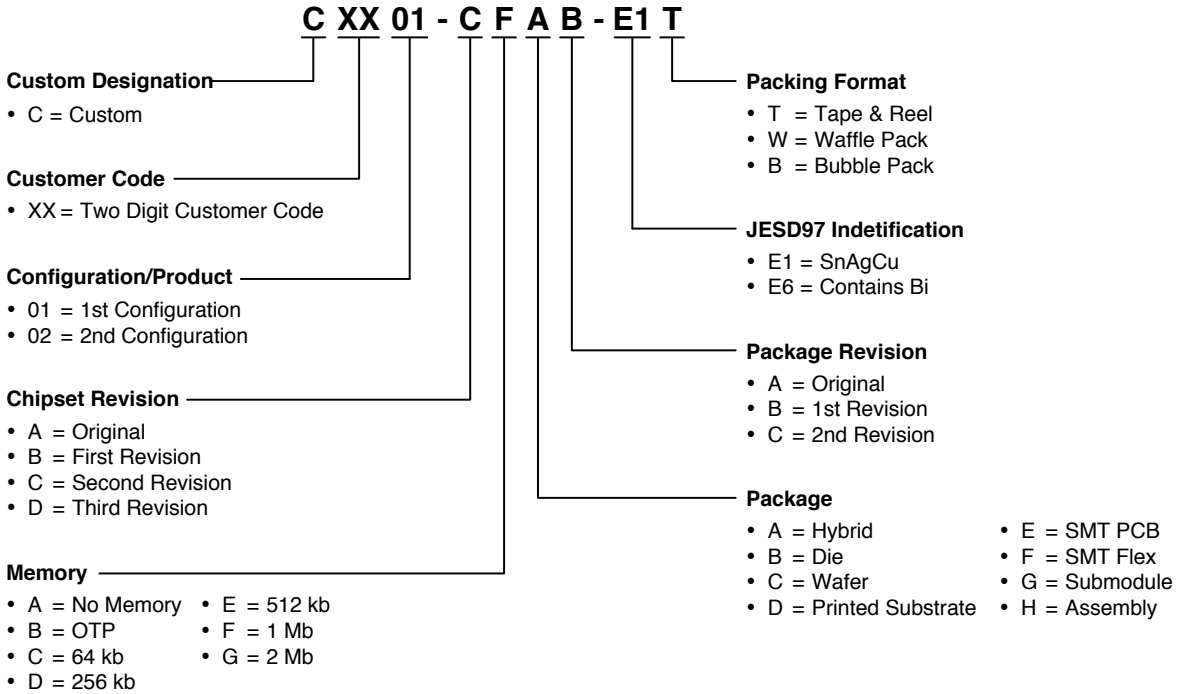
Chromaticity
- C = RGB (Red, Green, Blue)
- M = Monochrome
- R = Red/Clear
- G = RGBC
- Y = CMY (Cyan, Magenta, Yellow)
- L = Logic - IP "00"

Operating Temp
- ST = Commercial
- AT = Automotive
- XT = Extended

Naming Convention for Preconfigured Hearing Products



Naming Convention for Custom Hearing Products



Naming Convention for Ezairo-Based Hybrid Products

E 71 60 - 1 P - 1 01 WD 57 - A G

Family Designation
- E = EZAIRO

Series
- 59 = Ezairo 5900 Family
- 62 = Ezairo 6200 Family
- 71 = Ezairo 7100 Family

Configuration
- 01 = 1st Package
- 02 = 2nd Package
- 30 = 3rd Package
- 40 = 4th Package
- 50 = 5th Package
- 60 = 6th Package

Hybrid Version
- 0 = First
- 1 = Second

MFi Capable (For Ezairo 7160 SL)
- P = MFi Support
- Blank = No MFi Support

Chip Version
- 1 = Rev 1

Chipset Revision (Major)
- 01 = 1st Revision
- 02 = 2nd Revision

Green
- G = Green
- L = Leaded

Carrier Type
- A = Tape & Reel (For Ezairo 7110 = MOQ 250)
- BP = Bubble Pack (MOQ 25)
- T = Trays
- U = Tubes
- W = Wafer Box

Number of Pins/Balls

Numeric Value

Package
- A = Hybrid
- B = BGA
- BD = Bumped Die
- D = DFN
- S = System in Package (SiP)
- WC = WLCSP with Backside Coating
- WC150 = WLCSP with Backside Coating, 150 μm
- WD = Wafer in Die Quantity
- Q = QFN
- W = WLCSP
- U = Unbumped Die

Naming Convention for Ezairo Die Products

E 83 00 - 1 01 WD 78 - A B G

Family Designation
- E = EZAIRO

Series
- 59 = Ezairo 5900 Family
- 62 = Ezairo 6200 Family
- 71 = Ezairo 7100 Family
- 83 = Ezairo 8300 Family

Configuration
- 00 = Die

Chip Version
- 1 = Rev 1

Chipset Revision (Major)
- 01 = 1st Revision
- 02 = 2nd Revision

Green
- G = Green
- L = Leaded

Qualification Type
- A = Medical, Life Threatening
- B = Medical, Non-Life Threatening
- C = Consumer

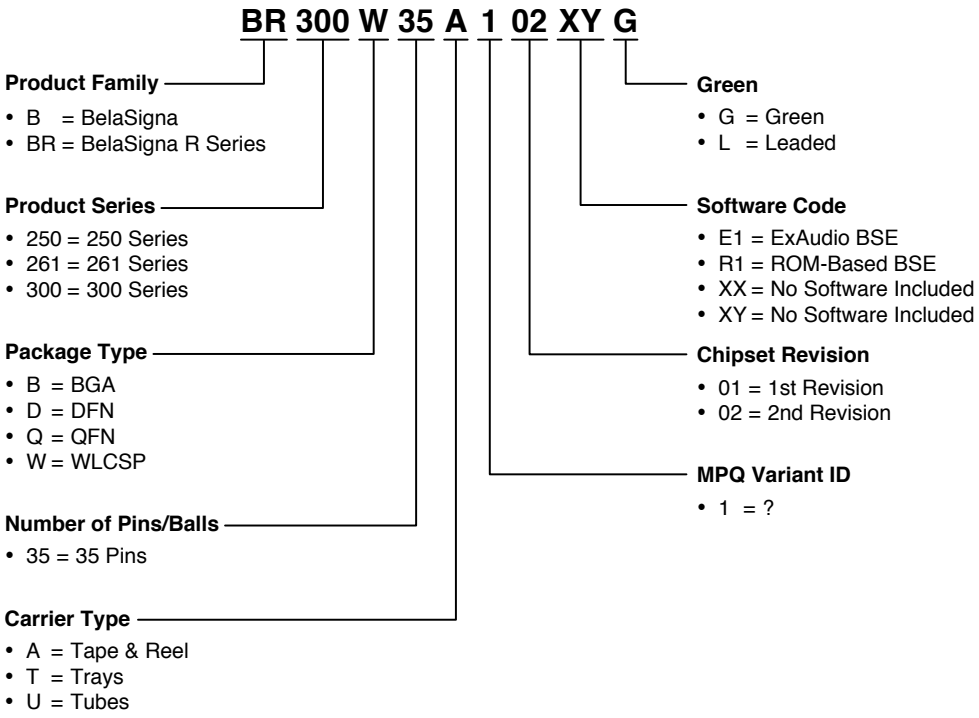
Carrier Type
- A = Tape & Reel
  - Ezairo 7100 = MOQ 5,000
- B = Tape & Reel
  - Ezairo 7100 = MOQ 500
- BP = Bubble Pack
  - MOQ 25
- T = Trays
- U = Tubes
- W = Wafer Box

Number of Pins/Balls

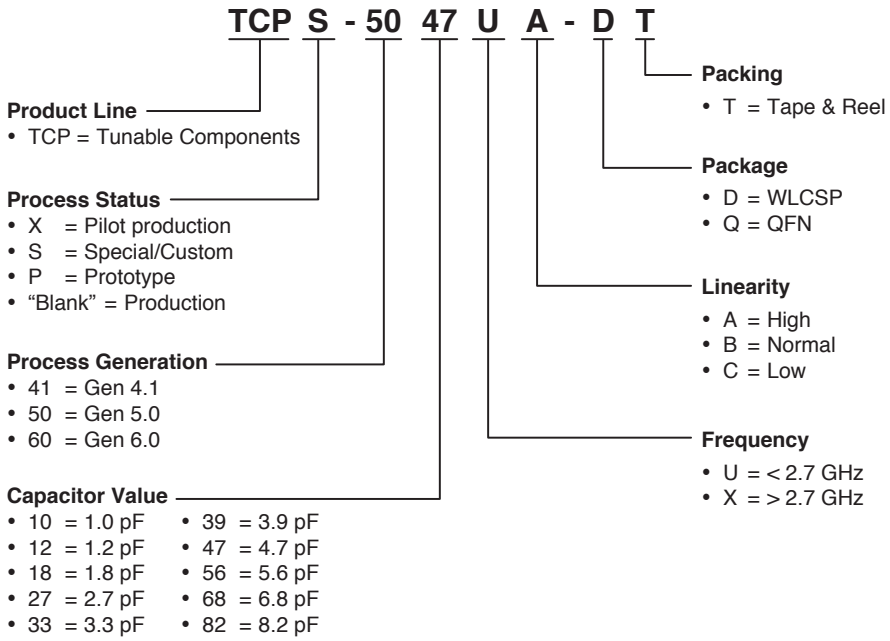
Numeric Value

Package
- A = Hybrid
- B = BGA
- BD = Bumped Die
- D = DFN
- S = System in Package (SiP)
- WC = WLCSP with Backside Coating
- WC150 = WLCSP with Backside Coating, 150 μm
- WD = Wafer in Die Quantity
- Q = QFN
- W = WLCSP
- U = Unbumped Die

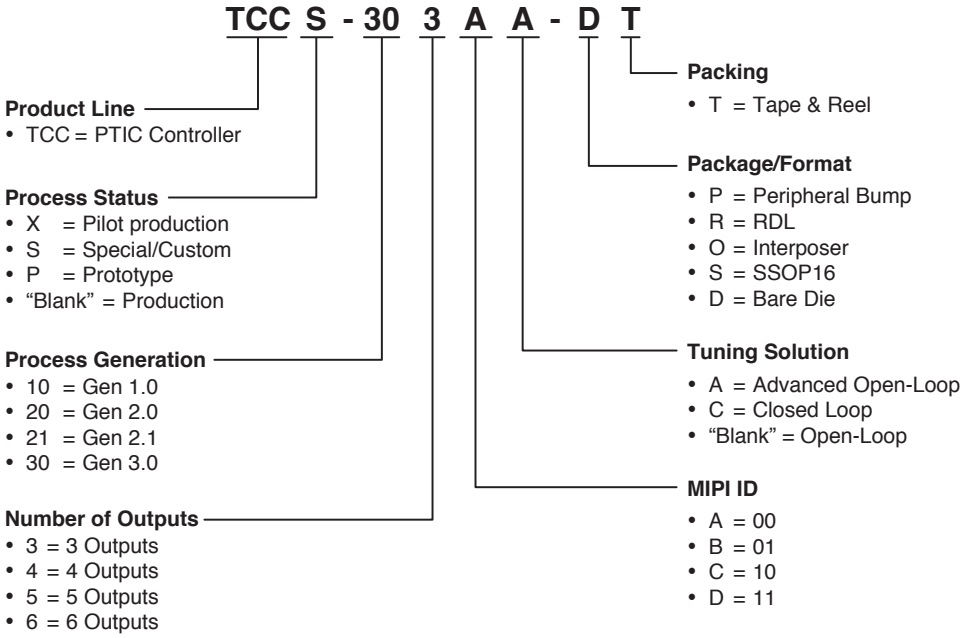
Naming Convention for BelaSigna Products



Naming Convention for Passive Tunable Integrated Circuits (PTIC)



Naming Convention for Passive Tunable Integrated Circuit (PTIC) Controllers



Naming Convention for Dual PTIC RF Tuner IC

TCP - 50 1 x - D T

Product Line
- TCP = Tunable Components

Process Generation
- 50 = Gen 5.0
- 60 = Gen 6.1

Product Variant
- 1 = 8.2 pF PTIC + 2.7 pF PTIC

Optional Suffix
- 'Blank' = Standard Part

Package
- D = WLCSP

Packing
- T = Tape & Reel

Naming Convention for Power Management ICs

HPM 10 01 - BD C C A - E1 T

Product Class
- HPM = Hearing Aid Power Management

Product Generation
- 10 = Contact-Based Version
  20 Wireless Version

Configuration/Product
- 01 = 1st Configuration
- 02 = 2nd Configuration

Package
- A = Hybrid
- B = BGA
- BD = Bumped Die
- D = DFN
- Q = WFN
- S = System in Package (SiP)
- U = Umbumped Die
- W = WLCSP
- WC = WLCSP with Backside Coating

Memory
- A = No Memory
- B = OTP
- C = 64 kb
- D = 256 kb
- E = 512 kb
- F = 1 Mb
- G = 2 Mb

Package
- A = Hybrid
- B = Die
- C = Wafer
- D = Printed Substrate
- E = SMT PCB
- F = SMT Flex
- G = Submodule
- H = Assembly

Package Revision
- A = Original
- B = 1st Revision
- C = 2nd Revision

JESD97 Indetification
- E1 = SnAgCu
- E6 = Contains Bi

Packing Format
- T = Tape & Reel
- W = Waffle Pack
- B = Bubble Pack

Naming Convention for Bluetooth® Low Energy RF ICs

NCH - RSL 10 - x 1 01 WC 51 - A B G

Product Class
- NCH-RSL = Consumer/Healthcare
- MD-RSL = Life Critical Devices
- NCV-RSL = Automotive

Product Generation
- 10 = Bluetooth 5.0

Special/Custom*
- 'Blank' = Standard

* Reserved for Special or Custom Designator

Chip Version
- 1 = 1st Version
- 2 = 2nd Version

Chip Revision (Major)
- 01 = 1st Revision
- 02 = 2nd Revision

Package
- G = Green
- L = Leaded

Qualification
- A = Medical – Life Threatening
- B = Medical – Non-Life Threatening
- C = Consumer

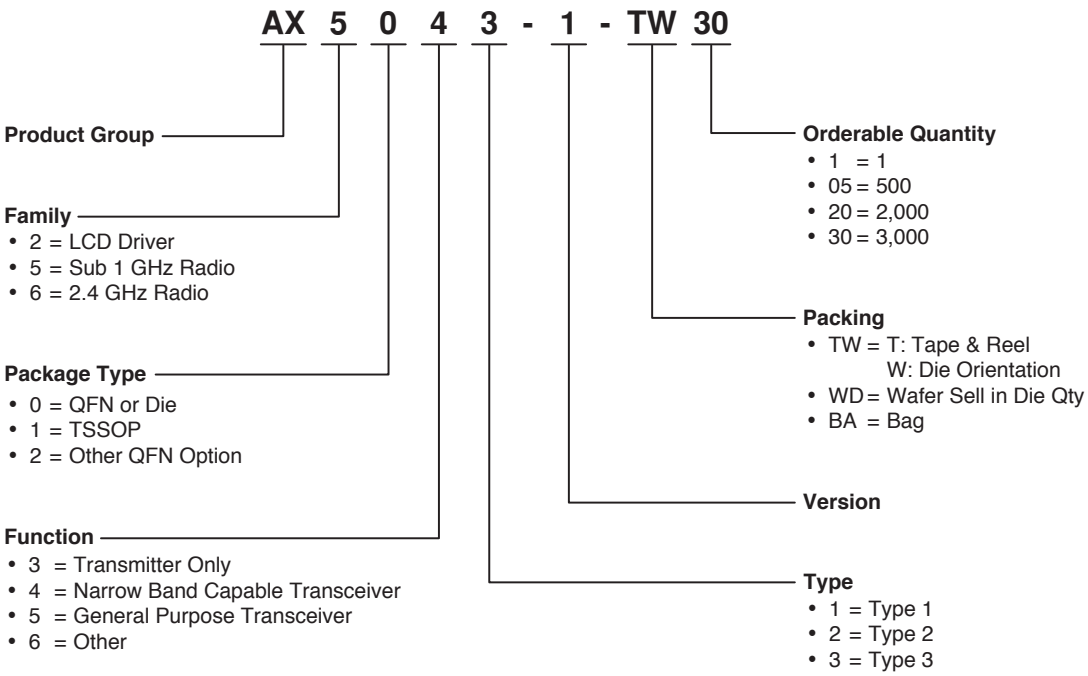
Carrier Type
- A = Tape & Reel
- T = Trays
- U = Tubes

Package Pins
- 51 = 51 Pins

Package
- A = Hybrid
- B = BGA
- BD = Bumped Die
- D = DFN
- Q = QFN
- S = System in Package (SiP)
- U = Unbumped Die
- W = WLCSP
- WC = WLCSP with Backside Coating

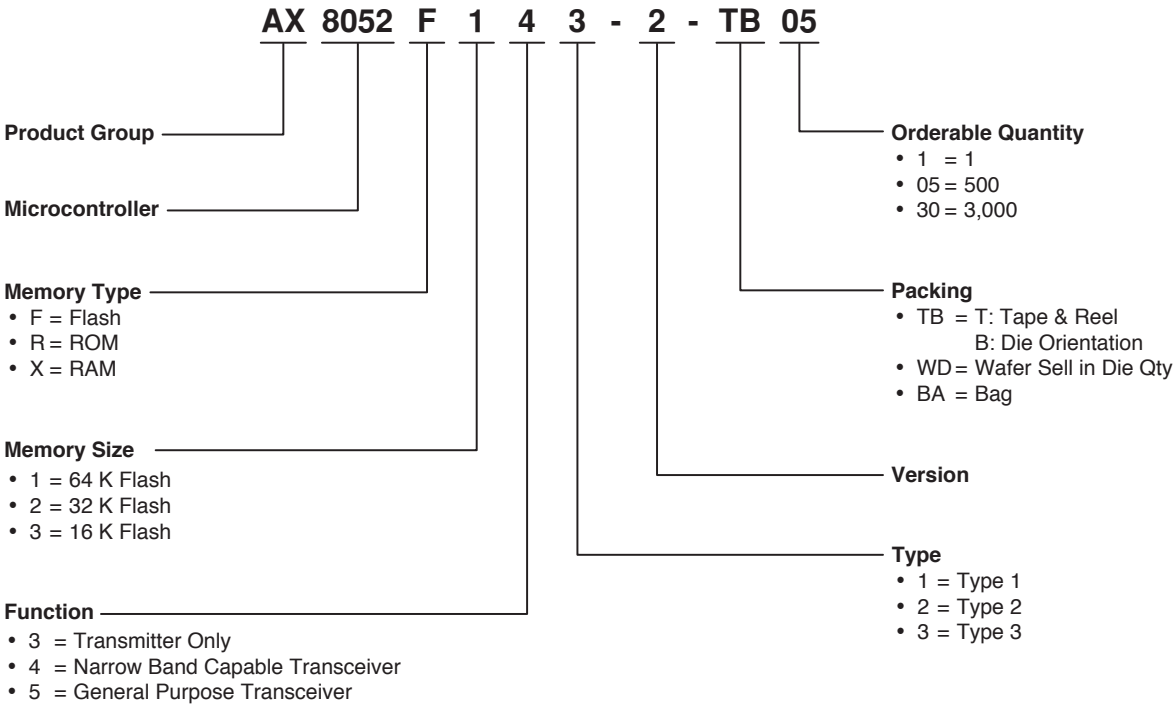
Naming Convention for Standard RF ICs

(Formerly Axsem)



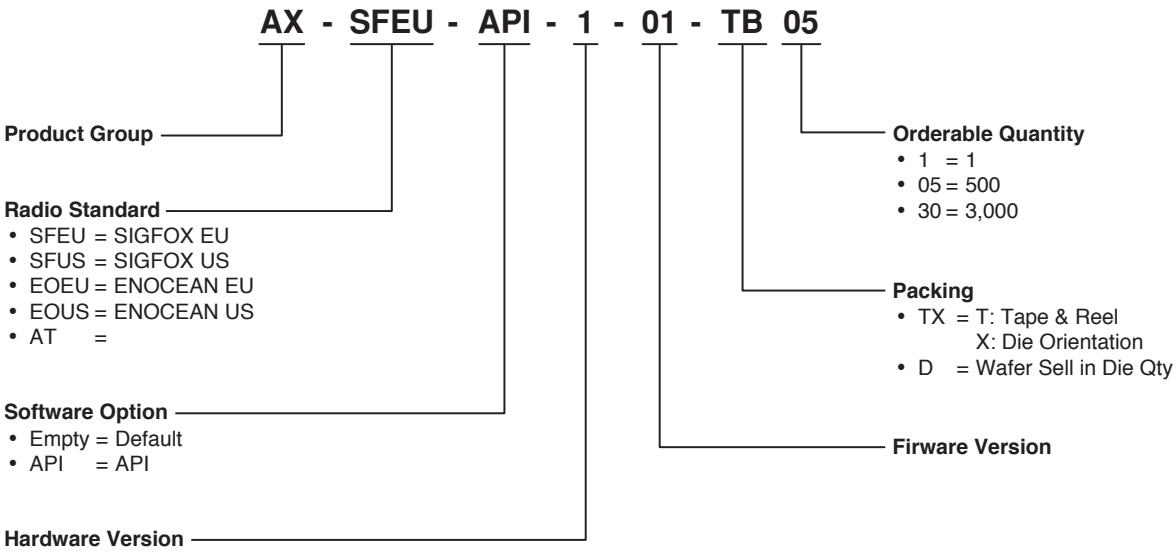
Naming Convention for RF Microcontrollers

(Formerly Axsem)



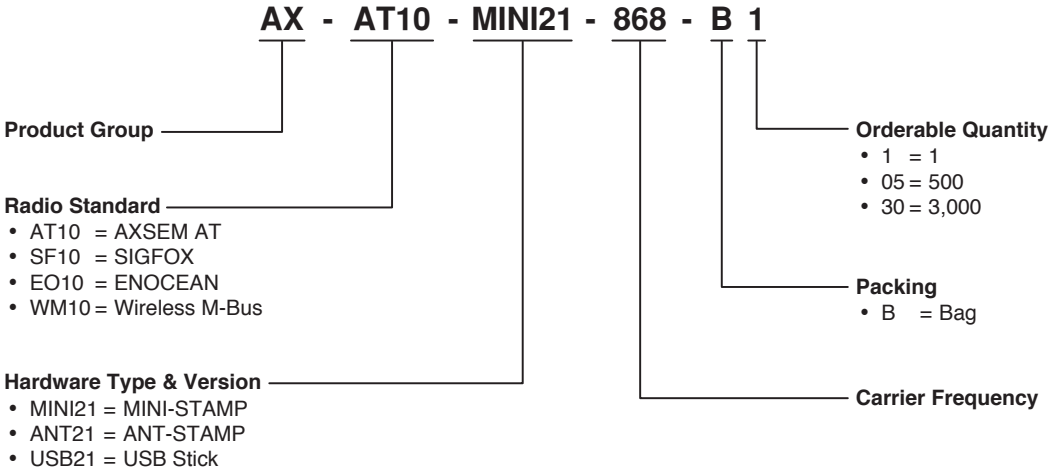
Naming Convention for RF Microcontrollers with Radio Standards

(Formerly Axsem)

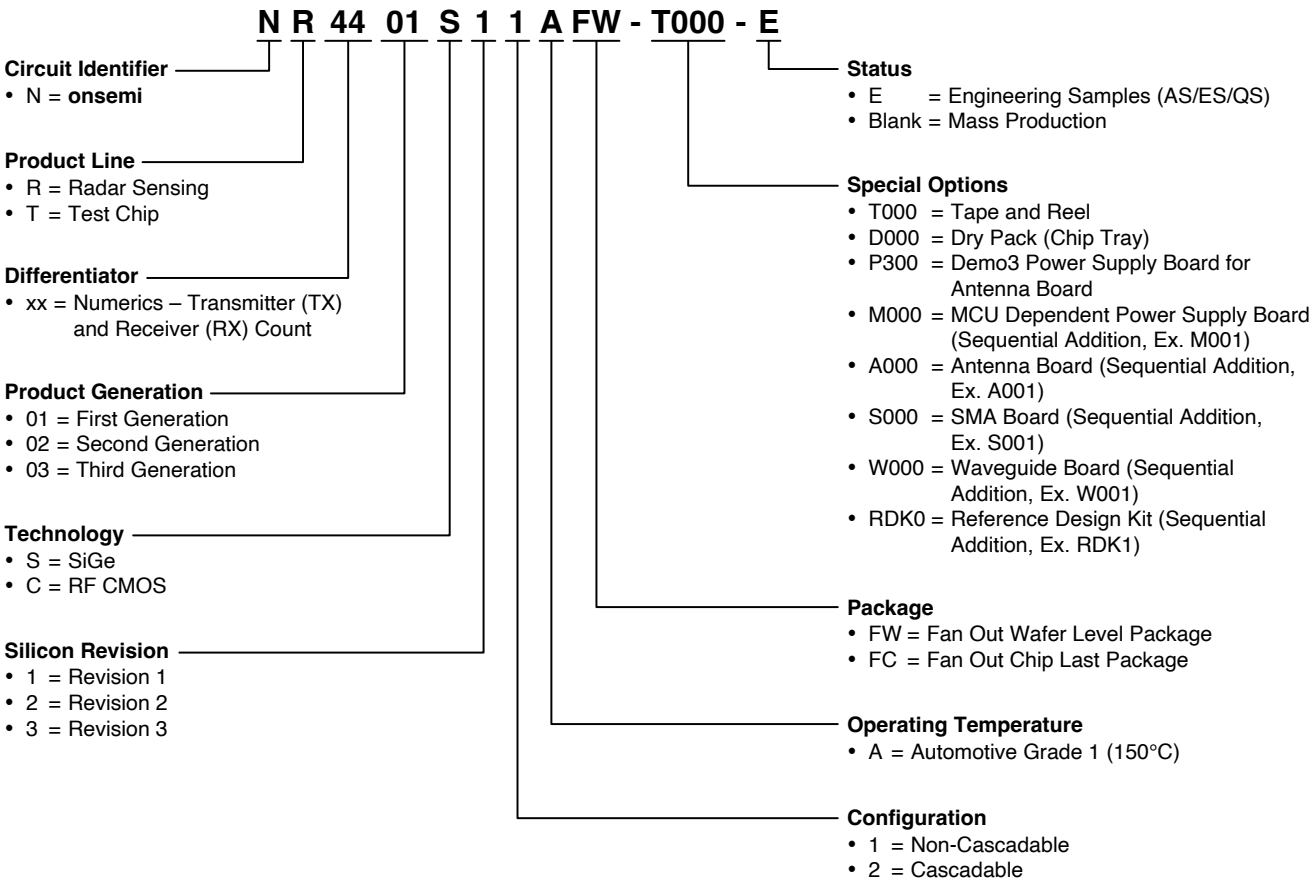


Naming Convention for RF Modules

(Formerly Axsem)



Naming Convention for Radar Products



Naming Convention for Single Pixel Silicon Photomultipliers

(Formerly SensL)

MICRO FC - 100 20 - SMT - TR - YYY - E XXX

Circuit Identifier
- MICRO = Single Pixel Sensor **onsemi**

Sensor Type
- FC = C-Series
- FJ = J-Series
- RB = RB-Series
- RD = RD-Series
- RDM = RDM-Series

Active Area
- 100 = 1.0 mm
- 300 = 3.0 mm
- 400 = 4.0 mm
- 600 = 6.0 mm

Microcell Size
- 10 = 10 μm
- 20 = 20 μm
- 35 = 35 μm
- 50 = 50 μm

Package Type
- SMT = MLP Package
- TSV = TSV Package
- MLP = MLP Package
- CSP = CSP Package

Packing
- TR = Full Reel (3,000 Pieces)
- TR1 = Partial Reel (1 to 2,999 Pieces)
- DR = Tray (-E Engineering Parts Only)

OPN Variant
- YYY = (Optional) Special Variant of OPN

Status
- Blank = Mass Production
- E = Engineering Samples

Mask Set Version
Numeric Value (Engineering Samples Only)

Naming Convention for Silicon Photomultiplier Arrays

(Formerly SensL)

ARRAY C - 100 20 - 64P - PCB - YYY - E XXX

Circuit Identifier
- ARRAY = SiPM Array **onsemi**

Sensor Type
- C = C-Series
- J = J-Series

Pixel Active Area
- 100 = 1.0 mm
- 300 = 3.0 mm
- 400 = 4.0 mm
- 600 = 6.0 mm

Microcell Size
- 10 = 10 μm
- 20 = 20 μm
- 35 = 35 μm
- 50 = 50 μm

Array Size
- 4P = 2 x 2 Pixels
- 16P = 4 x 4 Pixels
- 64P = 8 x 8 Pixels
- 122P = 12 x 12 Pixels

Connector Type
- BGA= Ball Grid Array
- PCB= Board-to-Board Connector

OPN Variant
- YYY = (Optional) Special Variant of OPN

Status
- Blank = Mass Production
- E = Engineering Samples

Mask Set Version
Numeric Value (Engineering Samples Only)

Naming Convention for LiDAR R-Series Silicon Photomultiplier Arrays

(Formerly SensL)

ARRAY RDM - XX YY A 20 - QFN - TR - YYY - E XXX

Circuit Identifier
- ARRAY = SiPM Array **onsemi**

Sensor Type
- RA = RA-Series
- RDM = RDM-Series

Number of Pixels in X Direction
Numeric Value

Number of Pixels in Y Direction
Numeric Value

Layout Variant
Alpha Character

Microcell Size
- 10 = 10 μm
- 20 = 20 μm
- 35 = 35 μm

Package Type
- DFN = DFN Package
- QFN = QFN Package
- BGA = iBGA Package
- CSP = CSP Package

Packing
- TR = Full Reel
- TR1 = Partial Reel
- DR = Tray (-E Engineering Parts Only)

OPN Variant
- YYY = (Optional) Special Variant of OPN

Status
- Blank = Mass Production
- E = Engineering Samples

Mask Set Version
Numeric Value (Engineering Samples Only)

Naming Convention for LiDAR SPAD Arrays

(Formerly SensL)

PAN - XXX YYY A - A A - QFN

Circuit Identifier
- PAN = Pandion SPAD Array

Number of Pixels in X Direction
Numeric Value

Number of Pixels in Y Direction
Numeric Value

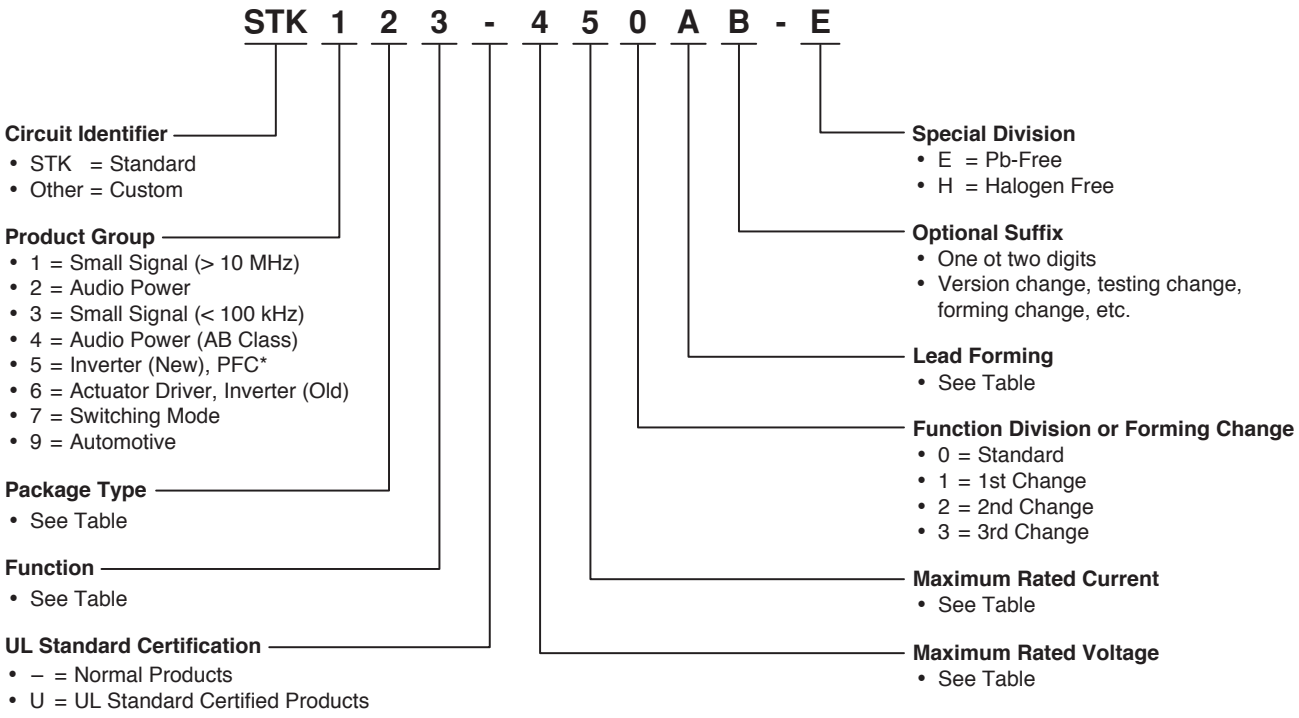
Unique Identifier
Alpha Character

Microcell Size
- A = Analog
- D = Digital
- M = Multiple

Temperature Grade
- C = Commercial (0 to +70°C)
- I = Industrial (-40 to +85°C)
- A = Automotive (-40 to +105°C)

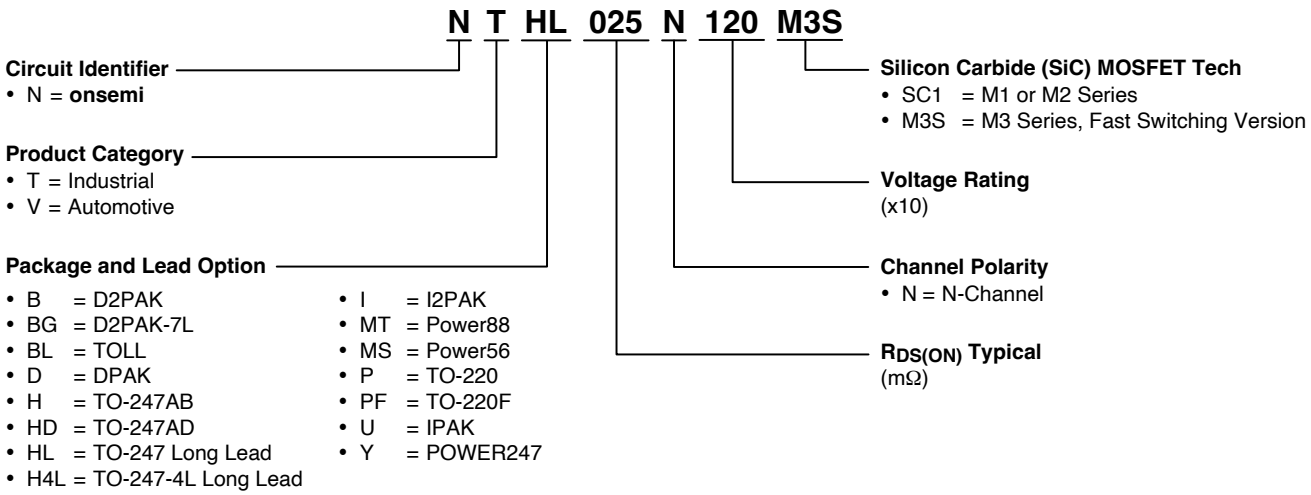
Package Type
- QFN = QFN Package

Naming Convention for IPM Devices

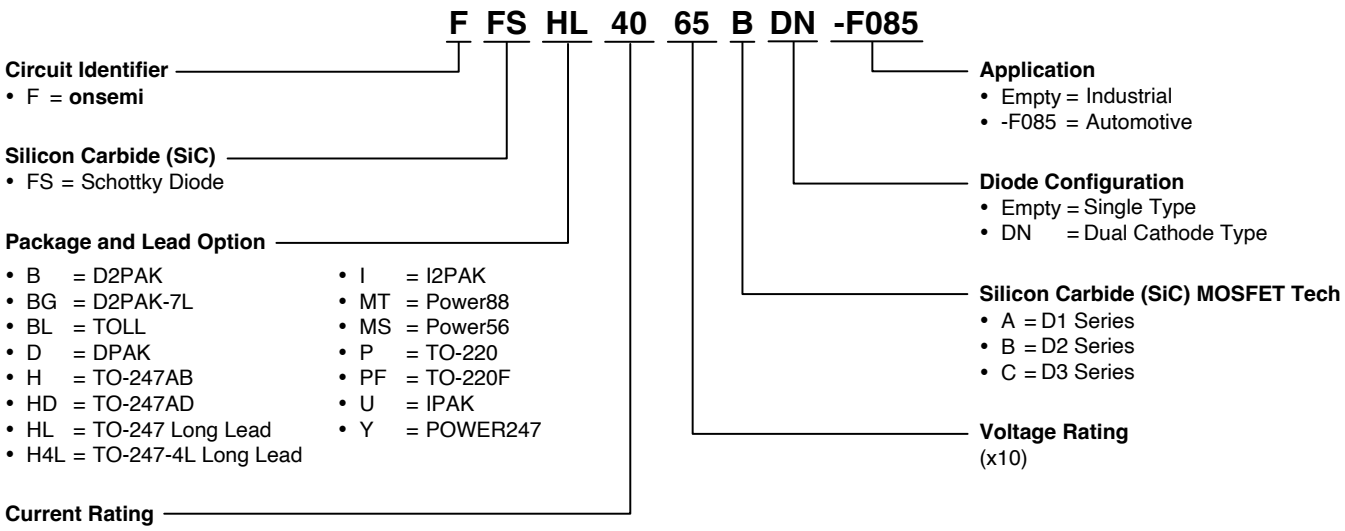


	2	3	4	5	A
Designator	Package Type	Function	Maximum Rated Voltage	Maximum Rated Current	Lead Forming
(Blank)	—	—	—	—	Straight
1	Smart	3-Phase Inverter; Built-In 1 Shunt R	Up to 150 V; Active High	1 A or Lower	—
2	Smart 2nd	3-Phase Inverter; For External 1 Shunt R	Up to 599 V; Active High	Up to 2 A	—
3	SIP04	3-Phase Inverter; Built-In 3 Shunt Rs	600 V; Active High	Up to 3 A	—
4	SOP1	3-Phase Inverter; For External 3 Shunt Rs	600 V; Active High	Up to 5 A	—
5	SIP1A	Single-Phase Inverter; Built-In 1 Shunt R	600 V; Active High	Up to 8 A	—
6	SIP2	Single-Phase Inverter; For External 1 Shunt R	Up to 1200 V; Active High	Up to 10 A	—
7	SIP2A	Induction Heating; 1 Burner	1700 V; Active High	Up to 10 A	—
8	SIP3	induction Heating; 2 Burners	—	Up to 12 A	—
9	SIP2 Case Type	PFC + 3-Phase Inverter	—	Up to 15 A	—
0	SIP3 Case Type	PFC + 3-Phase Inverter	—	Up to 15 A	—
A	DIP30	PFC; No Bridge	Up to 150 V; Active Low	Up to 20 A	SL Zigzag (From case to first clipping point = 2.5 mm)
B	DIP42	PFC; With Bridge	Up to 599 V; Active Low	Up to 25 A	SL Zigzag (From case to first clipping point = 5.35 mm)
C	DIPS	PFC; Bridge Free	600 V; Active Low	Up to 30 A	One Side Zigzag (Lead length 6.8 mm version)
D	DIP05	PFC; Interleave	600 V; Active Low	Up to 40 A	SL Bent
E	DIP2	PFC; Bridge Free Interleave	600 V; Active Low	Up to 50 A	One Side Zigzag (With insert plate)
F	DIP4	PFC + 3-Phase Inverter; No Bridge	Up to 1200 V; Active Low	Up to 60 A	L Bent
G	DIP5	PFC + 4-Phase Inverter; With Bridge	1700 V; Active Low	Up to 75 A	SL Bent + Stopper
H	Tenmen Case Screw	PFC + 5-Phase Inverter; Bridge Free	—	75 A or Larger	—
J	Tenmen Case Terminal	PFC + 6-Phase Inverter; Interleave	—	Up to 1 kW / 5 A	DIPS Bent (One side SL/One side SL Chidori; Lead length 5.5 mm version above case)
K	SIP2B	Power Conditioner; Converter	—	Up to 2 kW / 10 A	One Side Zigzag (Lead length 9 mm version)
L	DIPS2	Power Conditioner; Inverter	600 V	Up to 3 kW / 15 A	L-Zigzag (Smart 1st)
M	SIP3B	Power Conditioner; Converter + Inverter	600 V; Built-In 1 Shunt R	Up to 4 kW / 20 A	Both Side Chidori (Smart 2nd bent)
N	New Package	Power Conditioner; Others	600 V; Built-In HVIC	Up to 5 kW / 25 A	DIPS Bent (One side SL/One side SL Chidori; Lead length 9.7 mm version above case)
P	SIP3A	—	600 V; Built-In HVIC + Shunt R	Up to 6 kW / 30 A	—
Q	DIPS3	3-Phase Inverter + Break; Built-In a Shunt R	1200 V	Up to 8 kW / 40 A	—
R	DIPS3.5	3-Phase Inverter + Break; For External 3 Shunt Rs	1200 V; Built-In 1 Shunt R	Up to 10 kW	—
S	PQFN	CIB; Built-In a Shunt R	1200 V; Built-In HVIC	10 kW or Larger	—
T	SIP3A	CIB; For External 3 Shunt Rs	1200 V; Built-In HVIC + Shunt R	Up to 100 A	—
U	DIP-C2	—	—	Up to 150 A	—
V	DIP-C3	—	—	Up to 200 A	—

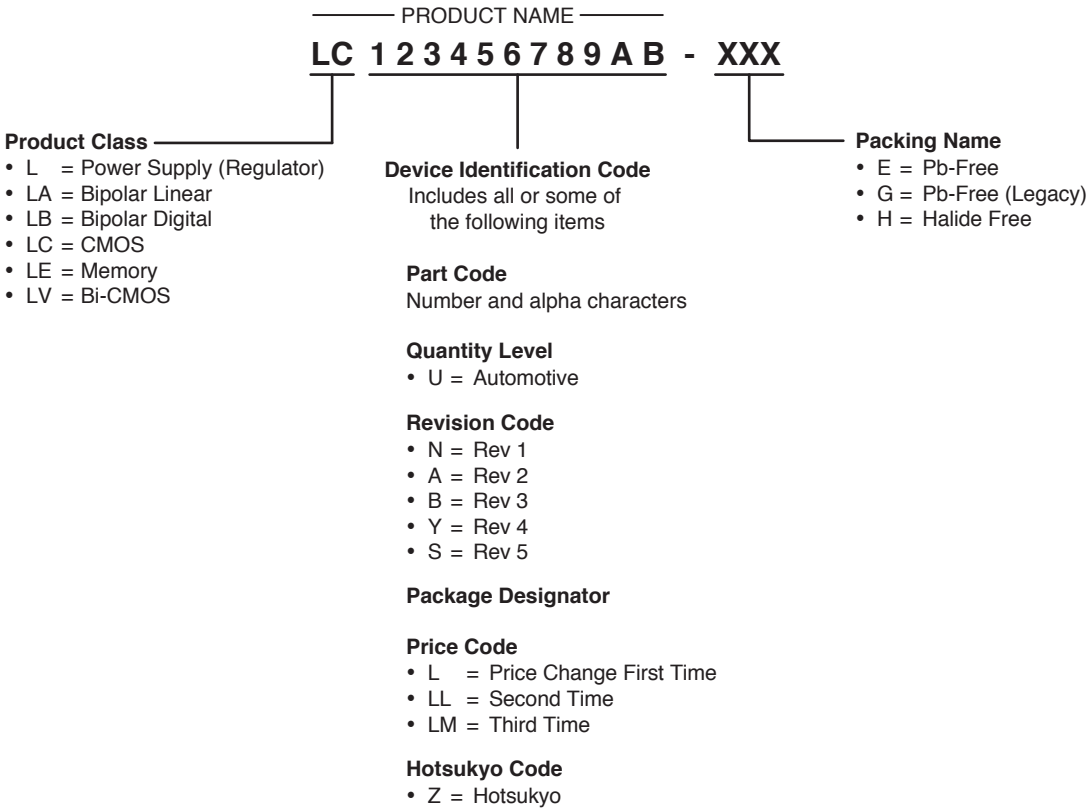
Naming Convention for SiC MOSFETs (EliteSiC)



Naming Convention for SiC Diodes (EliteSiC)



Naming Convention for DS and iPS Devices



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