STM32F10xx8 and STM32F10xxB Errata sheet

STM32F101x8/B, STM32F102x8/B and STM32F103x8/B medium-density device limitations

Silicon identification

This errata sheet applies to the revisions B, Z and Y of the STMicroelectronics medium-density STM32F101xx access line and STM32F103xx performance line products, and to revision Y of the STM32F102xx USB access line devices.
These families feature an ARM™ 32-bit Cortex®-M3 core, for which an errata notice is also available (see *Section 1* for details).

The full list of root part numbers is shown in *Table 2*.

The products are identifiable as shown in *Table 1*:

- by the Revision code marked below the Sales Type on the device package
- by the last three digits of the Internal Sales Type printed on the box label

Table 1. Device identification(1)

Sales type	Revision code(2) marked on device
STM32F101xxx(3)	“B”, “Z” or “Y”
STM32F102xxx(3)	“Y”
STM32F103xxx(3)	“B”, “Z” or “Y”

1. The REV_ID bits in the DBGMCU_IDCODE register show the revision code of the device (see the STM32F10xxx reference manual for details on how to find the revision code).
2. Refer to *Appendix A: Revision code on device marking* for details on how to identify the Revision code on the different packages.
3. Are also concerned all devices with 32 KB of Flash memory that do not have the letter A in their sales type.

Table 2. Device summary

Reference	Part number
STM32F101xx	STM32F101C8, STM32F101R8 STM32F101V8, STM32F101T8
	STM32F101RB, STM32F101VB, STM32F101CB
STM32F102xx	STM32F102C8, STM32F102R8
	STM32F102CB, STM32F102RB
STM32F103xx	STM32F103C8, STM32F103R8 STM32F103V8, STM32F103T8
	STM32F103RB STM32F103VB, STM32F103CB

1 ARM™ 32-bit Cortex®-M3 limitations

An errata notice of the STM32F10xxx core is available from the following web address: *http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.eat0420a/*.
The direct link to the errata notice pdf is:
http://infocenter.arm.com/help/topic/com.arm.doc.eat0420a/Cortex-M3-Errata-r1p1-v0.2.pdf.
All the described limitations are minor and related to the revision r1p1-01rel0 of the Cortex-M3 core.

2 STM32F10xxx silicon limitations

2.1 Voltage glitch on ADC input 0

Description

A low-amplitude voltage glitch may be generated (on ADC input 0) on the PA0 pin, when the ADC is converting with injection trigger. It is generated by internal coupling and synchronized to the beginning and the end of the injection sequence, whatever the channel(s) to be converted.

The glitch amplitude is less than 150 mV with a typical duration of 10 ns (measured with the I/O configured as high-impedance input and left unconnected). If PA0 is used as a digital output, this has no influence on the signal. If PA0 is used has a digital input, it will not be detected as a spurious transition, providing that PA0 is driven with an impedance lower than 5 kΩ. This glitch does not have any influence on the remaining port A pin or on the ADC conversion injection results, in single ADC configuration.

When using the ADC in dual mode with injection trigger, and in order to avoid any side effect, it is advised to distribute the analog channels so that Channel 0 is configured as an injected channel.

Workaround

None.

2.2 Flash memory read after WFI/WFE instruction

Conditions

- Flash prefetch on
- Flash memory timing set to 2 wait states
- FLITF clock stopped in Sleep mode

Description

If a WFI/WFE instruction is executed during a Flash memory access and the Sleep duration is very short (less than 2 clock cycles), the instruction fetch from the Flash memory may be corrupted on the next wakeup event.

Workaround

When using the Flash memory with two wait states and prefetch on, the FLITF clock must *not* be stopped during the Sleep mode – the FLITFEN bit in the RCC_AHBENR register must be set (keep the reset value).

2.3 Debug registers cannot be read by user software

Description

The DBGMCU_IDCODE and DBGMCU_CR debug registers are accessible only in debug mode (not accessible by the user software). When these registers are read in user mode, the returned value is 0x00.

Workaround

None.

2.4 Alternate function

In some specific cases, some potential weakness may exist between alternate functions mapped onto the same pin.

2.4.1 USART1_RTS and CAN_TX

Conditions

- USART1 is clocked
- CAN is not clocked
- I/O port pin PA12 is configured as an alternate function output.

Description

Even if CAN_TX is not used, this signal is set by default to 1 if I/O port pin PA12 is configured as an alternate function output.

In this case USART1_RTS cannot be used.

Workaround

When USART1_RTS is used, the CAN must be remapped to either another IO configuration when the CAN is used, or to the unused configuration (CAN_REMAP[1:0] set to “01”) when the CAN is not used.

2.4.2 SPI1 in slave mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal), if SPI1 is used in slave mode.

Workaround

None.

2.4.3 SPI1 in master mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal) if SPI1 is used in master mode and SP1_NSS is configured in software mode. In this case USART2_CK is not output on the pin.

Workaround

In order to output USART2_CK, the SSOE bit in the SPI1_CR2 register must be set to configure the pin in output mode.

2.4.4 SPI2 in slave mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in slave mode.

Workaround

None.

2.4.5 SPI2 in master mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in master mode and SP2_NSS is configured in software mode. In this case USART3_CK is not output on the pin.

Workaround

In order to output USART3_CK, the SSOE bit in the SPI2_CR2 register must be set to configure the pin in output mode,

2.4.6 I2C2 with SPI2 and USART3

Conditions

- I2C2 and SPI2 are clocked together or I2C2 and USART3 are clocked together
- I/O port pin PB12 is configured as an alternate function output

Description

- Conflict between the I2C2 SMBALERT signal (even if this function is not used) and SPI2_NSS in output mode.
- Conflict between the I2C2 SMBALERT signal (even if this function is not used) and USART3_CK.
- In these cases the I/O port pin PB12 is set to 1 by default if the I/O alternate function output is selected and I2C2 is clocked.

Workaround

I2C2 SMBALERT can be used as an output if SPI2 is configured in master mode with NSS in software mode.
I2C2 SMBALERT can be used in input mode if SPI2 is configured in master or slave mode with NSS managed by software.
SPI2 cannot be used in any other configuration when I2C2 is being used.

USART3 must *not* be used in synchronous mode when I2C2 is being used.

2.4.7 I2C1 with SPI1 remapped and used in master mode

Conditions

- I2C1 and SPI1 are clocked.
- SPI1 is remapped.
- I/O port pin PB5 is configured as an alternate function output.

Description

Conflict between the SPI1 MOSI signal and the I2C1 SMBALERT signal (even if SMBALERT is not used).

Workaround

Do not use SPI1 remapped in master mode and I2C1 together.

When using SPI1 remapped, the I2C1 clock must be disabled.

2.4.8 I2C1 and TIM3_CH2 remapped

Conditions

- I2C1 and TIM3 are clocked.
- I/O port pin PB5 is configured as an alternate function output.

Description

Conflict between the TIM3_CH2 signal and the I2C1 SMBALERT signal, (even if SMBALERT is not used).

In these cases the I/O port pin PB5 is set to 1 by default if the I/O alternate function output is selected and I2C1 is clocked. TIM3_CH2 cannot be used in output mode.

Workaround

To avoid this conflict, TIM3_CH2 can only be used in input mode.

2.5 PVD and USB wakeup events

Description

PVD and USB Wakeup, which are internally linked to EXTI line16 and EXTI line18, respectively, cannot be used as event sources for the Cortex-M3 core. As a consequence, these signals cannot be used to exit the Sleep or the Stop mode (exit WFE).

Workaround

Use interrupt sources and the WFI instruction if the application must be woken up from the Sleep or the Stop mode by PVD or USB Wakeup.

2.6 Compatibility issue with latest compiler releases

Description

Compilers with improved optimizations for the STM32F10xxx have been recently released on the market. Revisions Z and B of the medium-density STM32F10xxx devices (STM32F10xx8/B) do not support some of the sequences associated with the high-level optimizations done in these compilers. Revision Y is not affected by this limitation.

Workaround

This behavior is fully deterministic, and should be detected during firmware development or the validation phase. Consequently, systems already developed, validated and delivered to the field with previous silicon revisions are not affected.

For code update of revision Z and B devices already in the field, do not use these new compilers. To date, compilers known to generate these sequences are:

- IAR EWARM rev 5.20 and later
- GNU rev 4.2.3 and later

For new developments associated with these compilers, revision Y of the STM32F10xx8/B must be used.

Appendix A Revision code on device marking

Figure 1, *Figure 2*, *Figure 3*, *Figure 4* and *Figure 5* show the marking compositions for the LFBGA100, LQFP100, LQFP64, LQFP48 and VFQFPN36 packages, respectively. Only the Additional field containing the Revision code is shown.

Figure 1. LFBGA100 top package view

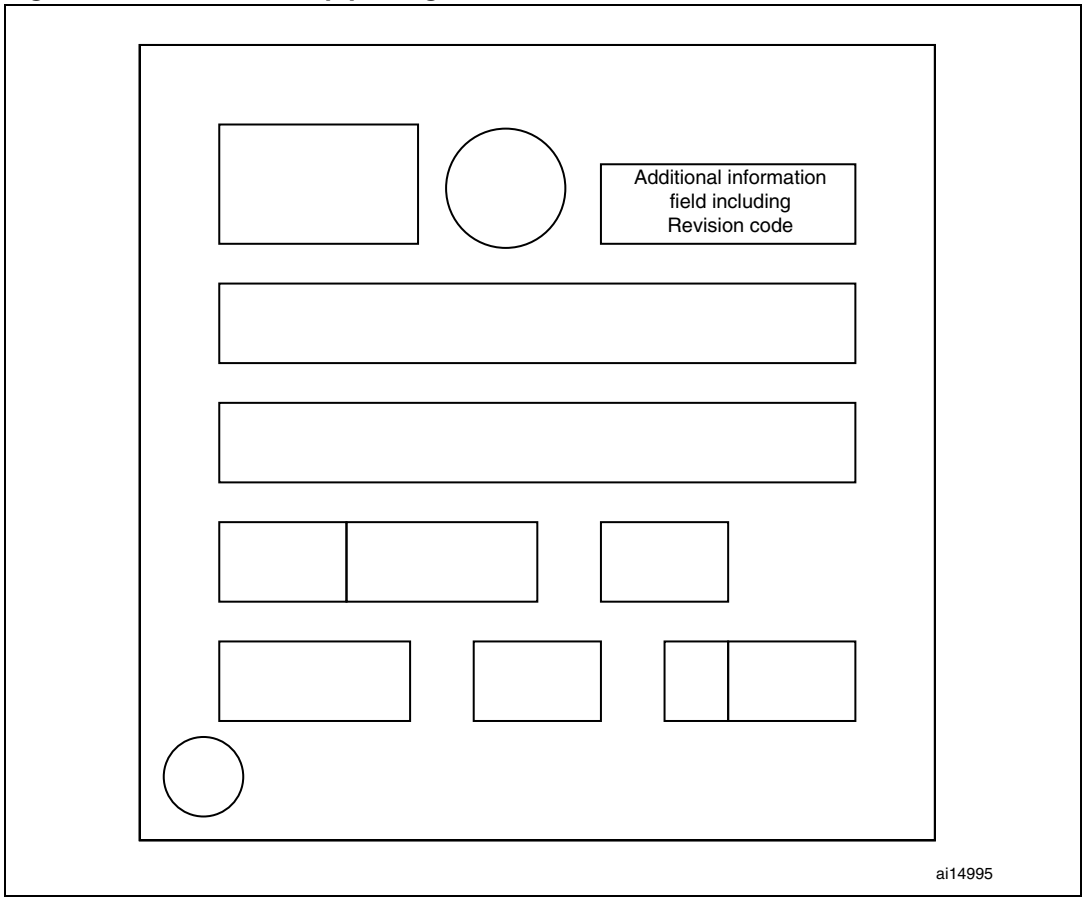


Figure 2. LQFP100 top package view

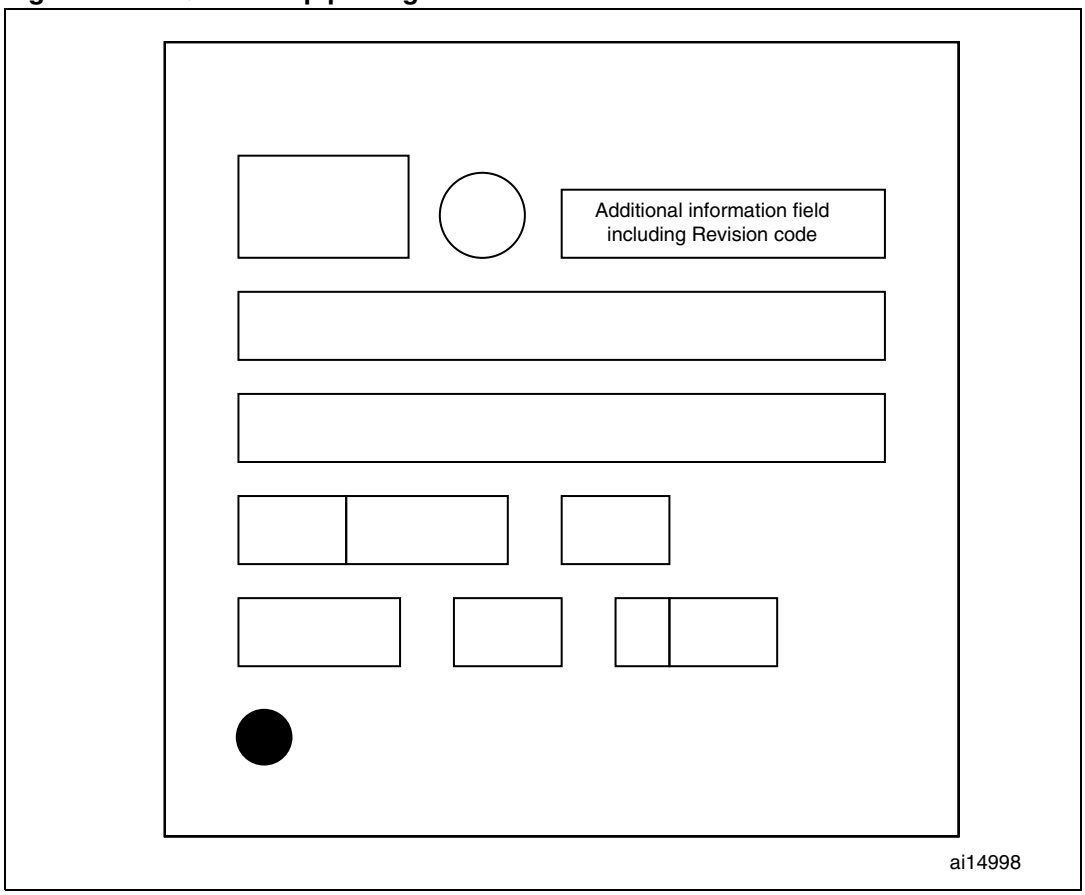


Figure 3. LQFP64 top package view

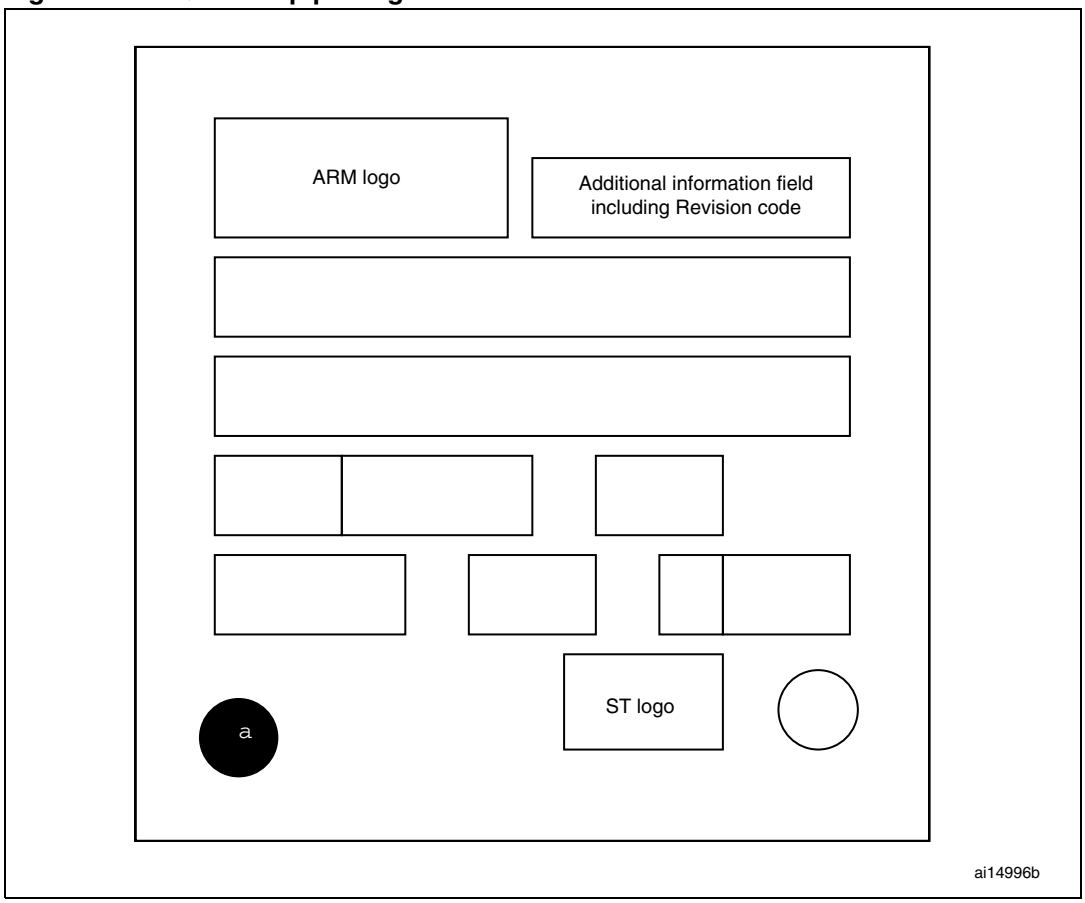


Figure 4. LQFP48 top package view

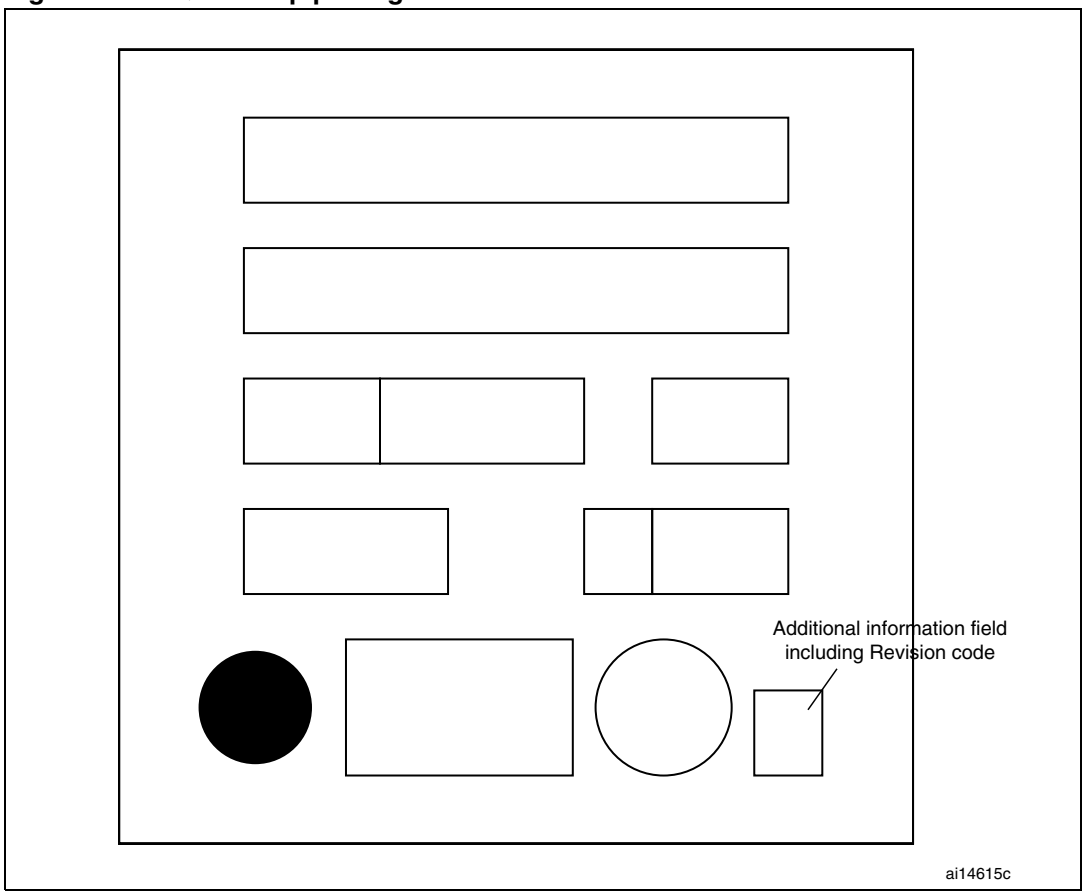
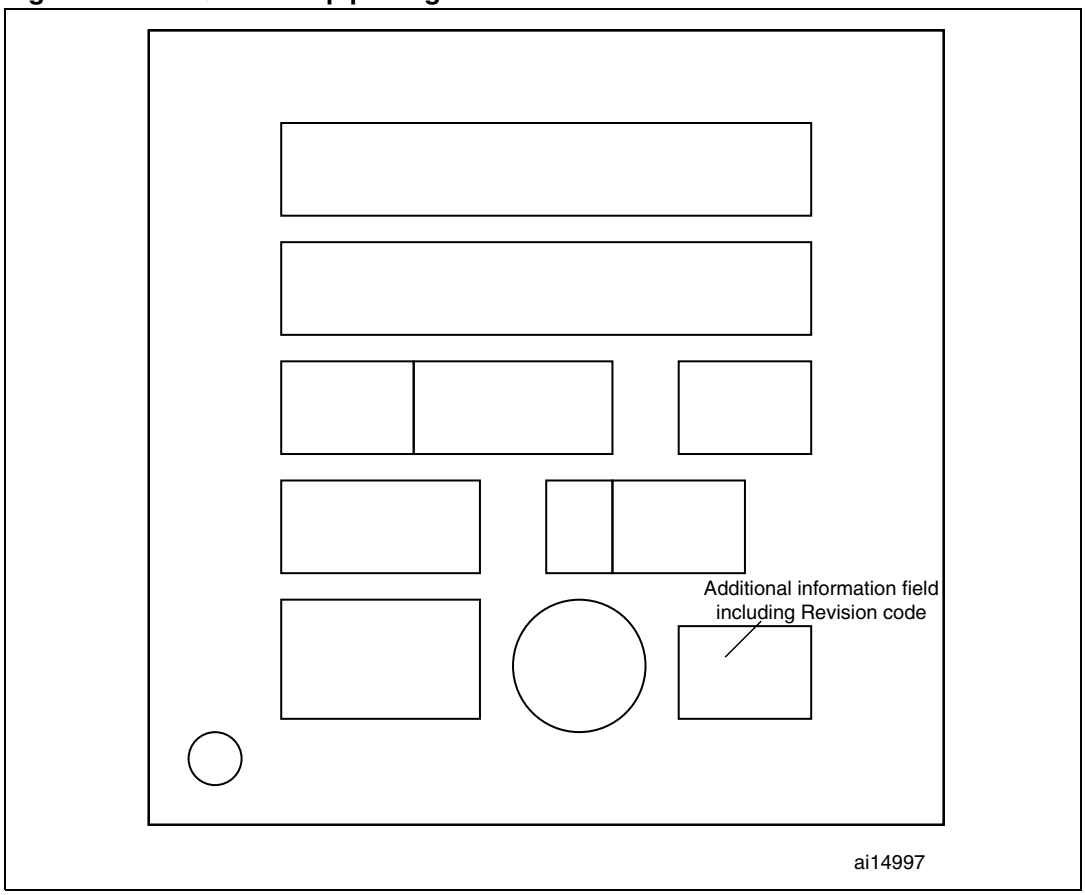


Figure 5. VFQFPN36 top package view



Revision history

Table 3. Document revision history

Date	Revision	Changes
28-Mar-2008	1	Initial release.
07-Apr-2008	2	*Section 2.2: Flash memory read after WFI/WFE instruction on page 2* added. Workaround specified in *Section 2.4.1: USART1_RTS and CAN_TX*.
23-May-2008	3	The errata sheet also applies to Revision Y devices. *Section 2.1: PD0 and PD1 use in output mode*, *Section 2.2: ADC auto-injection channel* and *Section 2.3: ADC combined injected simultaneous+interleaved* removed from errata sheet. *Section 2.3: Debug registers cannot be read by user software on page 3* added. Small text changes.
18-Jul-2008	4	*Section 2.5: PVD and USB wakeup events* added.
01-Oct-2008	5	This errata sheet also applies to STM32F102xx medium-density devices. Though medium-density devices with 32 Kbyte of Flash were removed, the errata sheet still applies to devices whose commercial code does not contain an “A”. *Section 2.6: Compatibility issue with latest compiler releases* added. *Figure 1: LFBGA100 top package view* added. *Figure 3: LQFP64 top package view* and *Figure 4: LQFP48 top package view* corrected.

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