



## **Introduction**

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use the High-density and Medium-density STM32F10xxx product families and describes the minimum hardware resources required to develop an STM32F10xxx application.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

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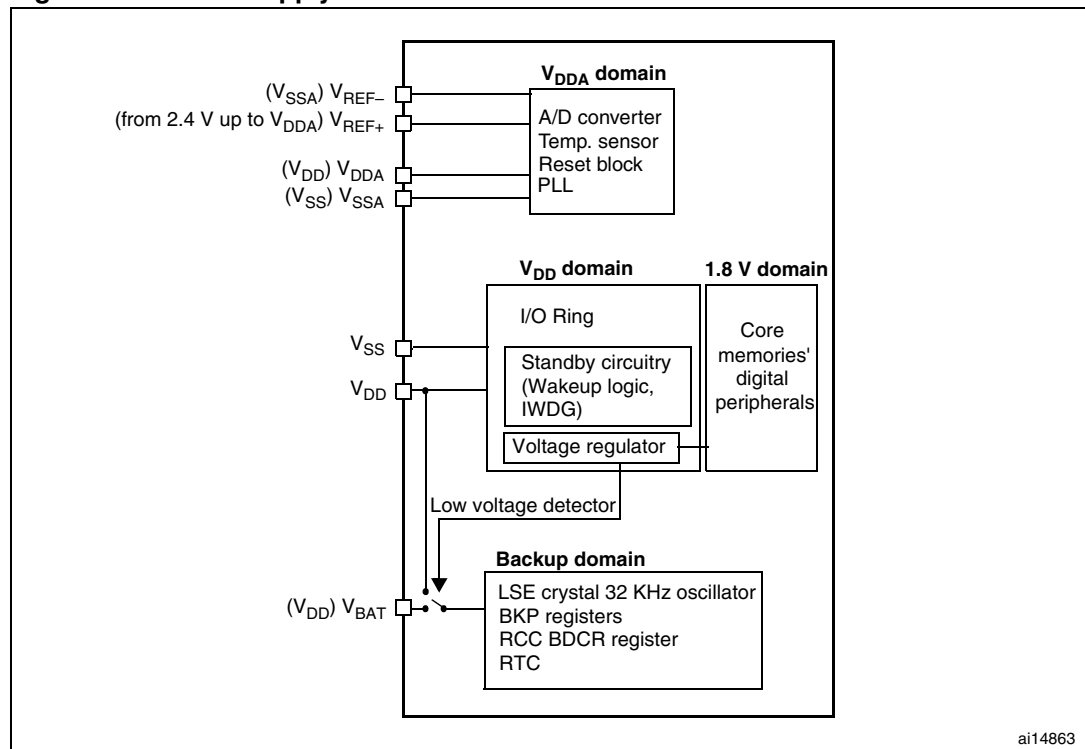
# 1 Power supplies

## 1.1 Introduction

The device requires a 2.0 V to 3.6 V operating voltage supply ( $V_{DD}$ ). An embedded regulator is used to supply the internal 1.8 V digital power.

The real-time clock (RTC) and backup registers can be powered from the  $V_{BAT}$  voltage when the main  $V_{DD}$  supply is powered off.

**Figure 1. Power supply overview**



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*Note:*  $V_{DDA}$  and  $V_{SSA}$  must be connected to  $V_{DD}$  and  $V_{SS}$ , respectively.

### 1.1.1 Independent A/D converter supply and reference voltage

To improve conversion accuracy, the ADC has an independent power supply that can be filtered separately, and shielded from noise on the PCB.

- the ADC voltage supply input is available on a separate  $V_{DDA}$  pin
- an isolated supply ground connection is provided on the  $V_{SSA}$  pin

When available (depending on package),  $V_{REF-}$  must be tied to  $V_{SSA}$ .

#### On 100-pin and 144-pin packages packages

To ensure a better accuracy on low-voltage inputs, the user can connect a separate external reference voltage ADC input on  $V_{REF+}$ . The voltage on  $V_{REF+}$  may range from 2.4 V to  $V_{DDA}$ .

### On packages with 64 pins or less

The  $V_{REF+}$  and  $V_{REF-}$  pins are not available, they are internally connected to the ADC voltage supply ( $V_{DDA}$ ) and ground ( $V_{SSA}$ ).

#### 1.1.2 Battery backup

To retain the content of the Backup registers when  $V_{DD}$  is turned off, the  $V_{BAT}$  pin can be connected to an optional standby voltage supplied by a battery or another source.

The  $V_{BAT}$  pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply ( $V_{DD}$ ) is turned off. The switch to the  $V_{BAT}$  supply is controlled by the power down reset (PDR) circuitry embedded in the Reset block.

If no external battery is used in the application,  $V_{BAT}$  must be connected externally to  $V_{DD}$ .

#### 1.1.3 Voltage regulator

The voltage regulator is always enabled after reset. It works in three different modes depending on the application modes.

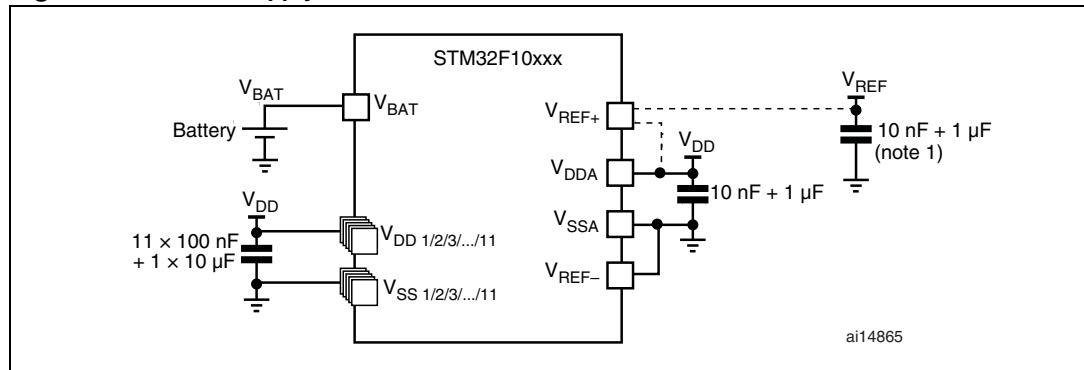
- in Run mode, the regulator supplies full power to the 1.8 V domain (core, memories and digital peripherals)
- in Stop mode, the regulator supplies low power to the 1.8 V domain, preserving the contents of the registers and SRAM
- in Standby mode, the regulator is powered off. The contents of the registers and SRAM are lost except for those concerned with the Standby circuitry and the Backup domain.

## 1.2 Power supply schemes

The circuit is powered by a stabilized power supply,  $V_{DD}$ .

- Caution:
  - If the ADC is used, the  $V_{DD}$  range is limited to 2.4 V to 3.6 V
  - If the ADC is not used, the  $V_{DD}$  range is 2.0 V to 3.6 V
- The  $V_{DD}$  pins must be connected to  $V_{DD}$  with external stabilization capacitors (eleven 100 nF ceramic capacitor + one Tantalum capacitor (min. 4.7  $\mu$ F typ. 10  $\mu$ F)).
- The  $V_{BAT}$  pin must be connected to the external battery (1.8 V <  $V_{BAT}$  < 3.6 V). if no external battery is used, this pin must be connected to  $V_{DD}$  with a 100 nF external ceramic stabilization capacitor.
- The  $V_{DDA}$  pin must be connected to two external stabilization capacitors (10 nF ceramic + 1  $\mu$ F Tantalum).
- The  $V_{REF+}$  pin can be connected to the  $V_{DDA}$  external power supply. If a separate, external reference voltage is applied on  $V_{REF+}$ , two 10 nF and 1  $\mu$ F capacitors must be connected on this pin. In all cases,  $V_{REF+}$  must be kept between 2.4 V and  $V_{DDA}$ .

**Figure 2. Power supply scheme**



1. Optional. If a separate, external reference voltage is connected on  $V_{REF+}$ , the two capacitors (10 nF and 1  $\mu$ F) must be connected.
2.  $V_{REF+}$  is either connected to  $V_{DDA}$  or to  $V_{REF-}$ .

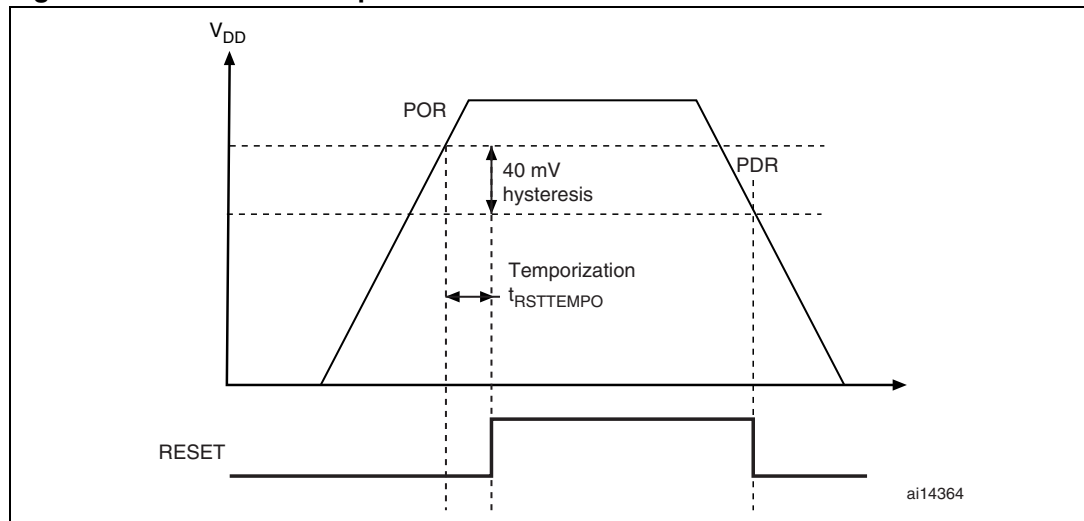
### 1.3 Reset & power supply supervisor

#### 1.3.1 Power on reset (POR) / power down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 2 V.

The device remains in the Reset mode as long as  $V_{DD}$  is below a specified threshold,  $V_{POR/PDR}$ , without the need for an external reset circuit. For more details concerning the power on/power down reset threshold, refer to the electrical characteristics in the STM32F101xx and STM32F103xx datasheets.

**Figure 3. Power on reset/power down reset waveform**





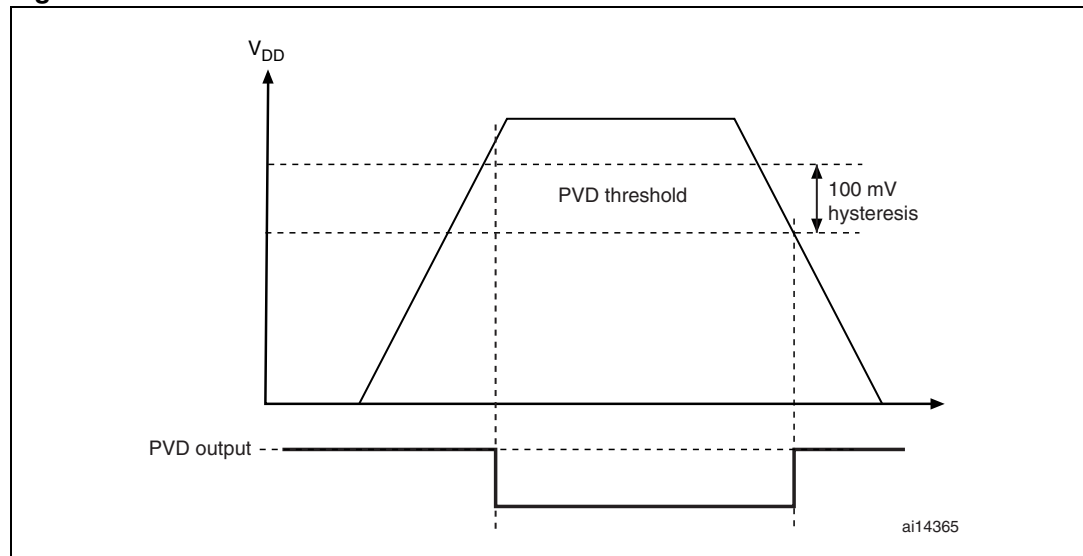
### 1.3.2 Programmable voltage detector (PVD)

You can use the PVD to monitor the  $V_{DD}$  power supply by comparing it to a threshold selected by the PLS[2:0] bits in the Power control register (PWR\_CR).

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the Power control/status register (PWR\_CSR), to indicate whether  $V_{DD}$  is higher or lower than the PVD threshold. This event is internally connected to EXTI Line16 and can generate an interrupt if enabled through the EXTI registers. The PVD output interrupt can be generated when  $V_{DD}$  drops below the PVD threshold and/or when  $V_{DD}$  rises above the PVD threshold depending on the EXTI Line16 rising/falling edge configuration. As an example the service routine can perform emergency shutdown tasks.

**Figure 4. PVD thresholds**



### 1.3.3 System reset

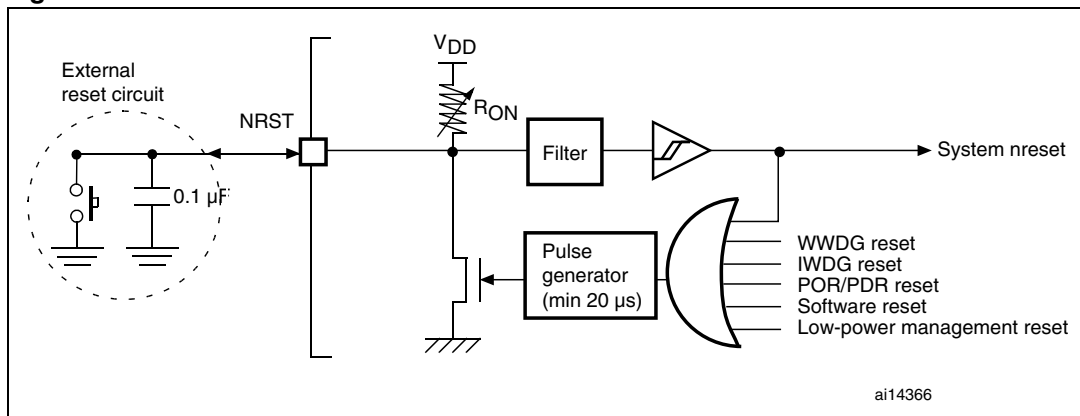
A system reset sets all registers to their reset values except for the reset flags in the clock controller CSR register and the registers in the Backup domain (see [Figure 1](#)).

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset)
2. window watchdog end-of-count condition (WWDG reset)
3. Independent watchdog end-of-count condition (IWDG reset)
4. A software reset (SW reset)
5. Low-power management reset

The reset source can be identified by checking the reset flags in the Control/Status register, RCC\_CSR.

Figure 5. Reset circuit



## 2 Clocks

Three different clock sources can be used to drive the system clock (SYSCLK):

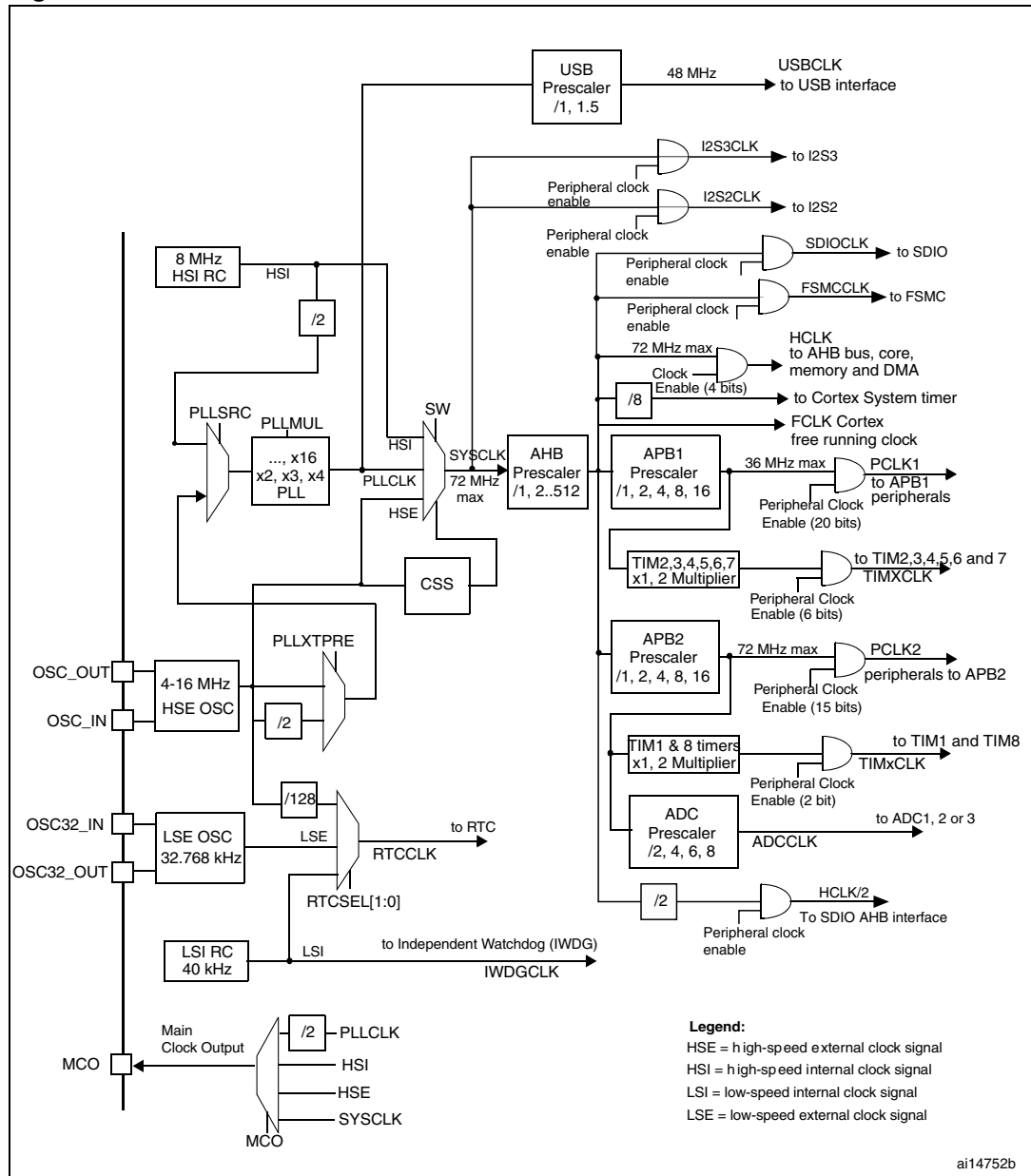
- HSI oscillator clock (high-speed internal clock signal)
- HSE oscillator clock (high-speed external clock signal)
- PLL clock

The devices have two secondary clock sources:

- 40 kHz low-speed internal RC (LSI RC) that drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the real-time clock (RTCCLK)

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption.

Figure 6. Clock overview



1. HSE = high-speed external clock signal; HSI = high-speed internal clock signal; LSI = low-speed internal clock signal; LSE = low-speed external clock signal.
2. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.

## 2.1 HSE OSC clock

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator (see [Figure 8](#))
- HSE user external clock (see [Figure 7](#))

Figure 7. External clock

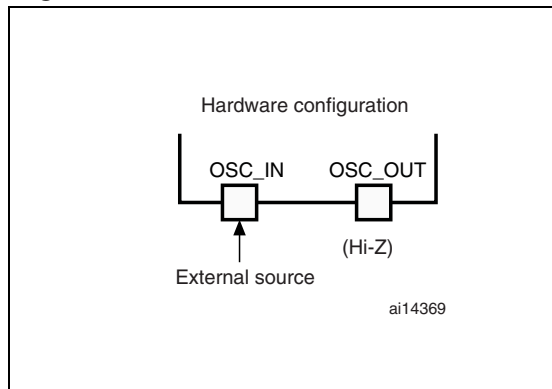
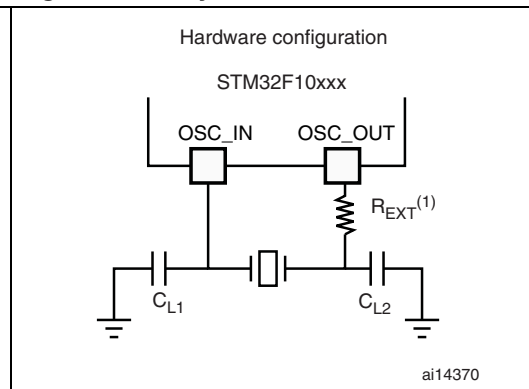


Figure 8. Crystal/ceramic resonators



1. The value of  $R_{EXT}$  depends on the crystal characteristics. Typical value is in the range of 5 to 6  $R_S$  (resonator series resistance).
2. Load capacitance  $C_L$  has the following formula:  $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$  where:  $C_{stray}$  is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Please refer to [Section 5: Recommendations on page 21](#) to minimize its value.

### 2.1.1 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 25 MHz. The external clock signal (square, sine or triangle) with a duty cycle of about 50%, has to drive the OSC\_IN pin while the OSC\_OUT pin must be left in the high impedance state (see [Figure 8](#) and [Figure 7](#)).

### 2.1.2 External crystal/ceramic resonator (HSE crystal)

The 4-to-16 MHz external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in [Figure 8](#).

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For  $C_{L1}$  and  $C_{L2}$  it is recommended to use high-quality ceramic capacitors in the 5 pF-to-25 pF range (typ.), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator.  $C_{L1}$  and  $C_{L2}$  are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of  $C_{L1}$  and  $C_{L2}$ . The PCB and MCU pin capacitances must be included when sizing  $C_{L1}$  and  $C_{L2}$  (10 pF can be used as a rough estimate of the combined pin and board capacitance).

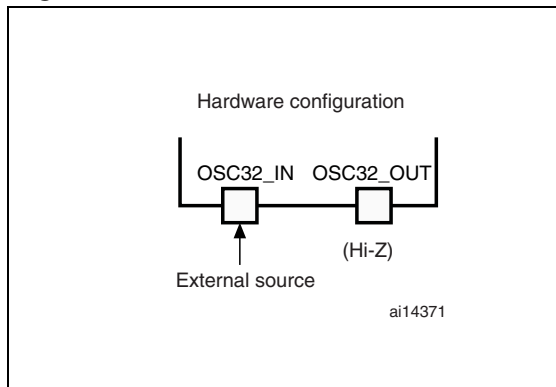
Refer to the electrical characteristics sections in the STM32F101xx and STM32F103xx datasheets for more details.

## 2.2 LSE OSC clock

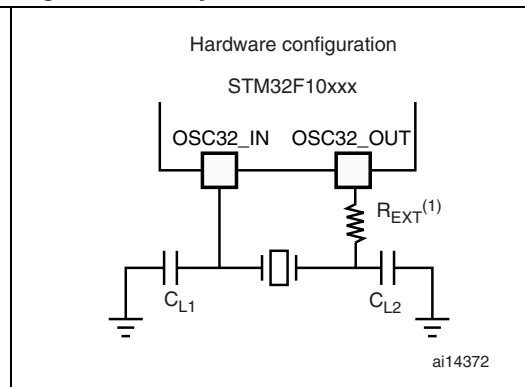
The low-speed external clock signal (LSE) can be generated from two possible clock sources:

- LSE external crystal/ceramic resonator (see [Figure 10](#))
- LSE user external clock (see [Figure 9](#))

**Figure 9. External clock**



**Figure 10. Crystal/ceramic resonators**



1. The value of  $R_{EXT}$  depends on the crystal characteristics.
2. OSC32\_IN and OSC\_OUT pins can be used also as GPIO, but it is recommended not to use them as both RTC and GPIO pins in the same application.

### 2.2.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It must have a frequency of 32.768 kHz. The external clock signal (square, sine or triangle) with a duty cycle of about 50% has to drive the OSC32\_IN pin while the OSC32\_OUT pin must be left high impedance (see [Figure 10](#) and [Figure 9](#)).

### 2.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It has the advantage of providing a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

## 2.3 Clock-out capability

The microcontroller clock output (MCO) capability allows the clock to be output onto the external MCO pin. The configuration registers of the corresponding GPIO port must be programmed in alternate function mode. One out of four clock signals can be selected as the MCO clock:

- SYSCLK
- HSI
- HSE
- PLL clock divided by 2

## 2.4 Clock security system (CSS)

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the HSE oscillator clock, the oscillator is automatically disabled. A clock failure event is sent to the break input of the TIM1 advanced control timer and an interrupt is generated to inform the software about the failure (clock security system interrupt CSSI), allowing the MCU to perform rescue operations. The CSSI is linked to the Cortex™-M3 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator is used directly or indirectly as the system clock (indirectly means that it is used as the PLL input clock, and the PLL clock is used as the system clock), a detected failure causes a switch of the system clock to the HSI oscillator and the disabling of the external HSE oscillator. If the HSE oscillator clock (divided or not) is the clock entry of the PLL used as system clock when the failure occurs, the PLL is disabled too.

For details, see the STM32F10xxx reference manual available from the STMicroelectronics website [www.st.com](http://www.st.com).

### 3 Boot configuration

#### 3.1 Boot mode selection

In the STM32F10xxx, three different boot modes can be selected by means of the BOOT[1:0] pins as shown in [Table 1](#).

**Table 1. Boot modes**

BOOT mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

This selection aliases the physical memory associated with each boot mode to Block 000 (boot memory). The values on the BOOT pins are latched on the 4<sup>th</sup> rising edge of SYSCLK after a reset. It is up to the user to set the BOOT1 and BOOT0 pins after reset to select the required boot mode.

The BOOT pins are also resampled when exiting the Standby mode. Consequently, they must be kept in the required Boot mode configuration in the Standby mode.

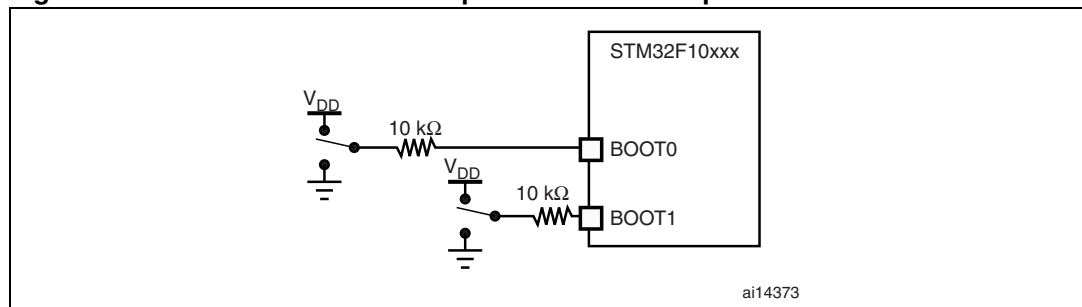
Even when aliased in the boot memory space, the related memory (Flash memory or SRAM) is still accessible at its original memory space.

After this startup delay has elapsed, the CPU starts code execution from the boot memory, located at the bottom of the memory address space starting from 0x0000\_0000.

#### 3.2 Boot pin connection

[Figure 11](#) shows the external connection required to select the boot memory of the STM32F10xxx.

**Figure 11. Boot mode selection implementation example**



1. Resistor values are given only as a typical example.



### 3.3 Embedded Boot Loader mode

The Embedded Boot Loader mode is used to reprogram the Flash memory using one of the serial interfaces (typically a UART). This program is located in the system memory and is programmed by ST during production.

For further details, please refer to Application note AN2606 available from the STMicroelectronics website, [www.st.com](http://www.st.com).

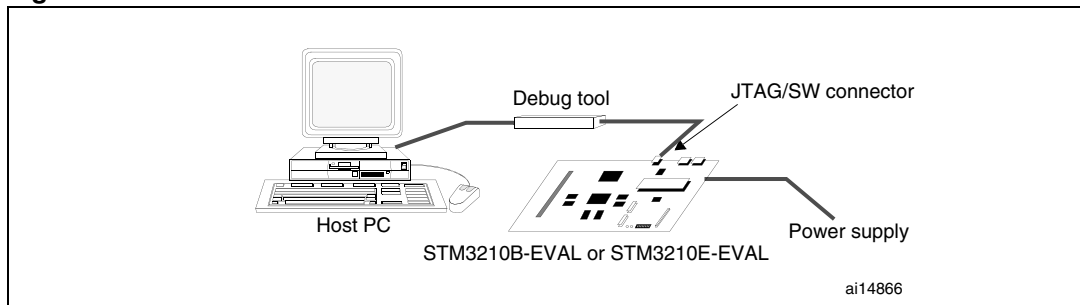
## 4 Debug management

### 4.1 Introduction

The Host/Target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG or SW connector and a cable connecting the host to the debug tool.

*Figure 12* shows the connection of the host to the evaluation board (STM3210B-EVAL board or STM3210E-EVAL board).

**Figure 12. Host-to-board connection**



### 4.2 SWJ debug port (serial wire and JTAG)

The STM32F10xxx core integrates the serial wire / JTAG debug port (SWJ-DP). It is an ARM® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

### 4.3 Pinout and debug port pins

The STM32F10xxx MCU is offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

#### 4.3.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as *alternate functions* of general-purpose I/Os (GPIOs). These pins, shown in *Table 2*, are available on all packages.

**Table 2. Debug port pin assignment**

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG Test Mode Selection	I/O	Serial Wire Data Input/Output	PA13
JTCK/SWCLK	I	JTAG Test Clock	I	Serial Wire Clock	PA14
JTDI	I	JTAG Test Data Input	-	-	PA15
JTDO/TRACESWO	O	JTAG Test Data Output	-	TRACESWO if async trace is enabled	PB3
JNTRST	I	JTAG Test nReset	-	-	PB4

### 4.3.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32F10xxx MCU implements a register to disable some part or all of the SWJ-DP port, and so releases the associated pins for general-purpose I/Os usage. This register is mapped on an APB bridge connected to the Cortex™-M3 system bus. This register is programmed by the user software program and not by the debugger host.

**Table 3. SWJ I/O pin availability**

Available Debug ports	SWJ I/O pin assigned				
	PA13 / JTMS / SWDIO	PA14 / JTCK / SWCLK	PA15 / JTDI	PB3 / JTDO	PB4 / JNTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without JNTRST	X	X	X	X	
JTAG-DP disabled and SW-DP enabled	X	X			
JTAG-DP disabled and SW-DP disabled	Released				

*Table 3* shows the different possibilities to release some pins.

For more details, see the STM32F10xxx reference manual, available from the STMicroelectronics website [www.st.com](http://www.st.com).

### 4.3.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must *not* be floating since they are directly connected to flip-flops to control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32F10xxx embeds internal pull-up and pull-down resistors on JTAG input pins:

- JNTRST: Internal pull-up
- JTDI: Internal pull-up
- JTMS/SWDIO: Internal pull-up
- TCK/SWCLK: Internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the equivalent state:

- JNTRST: Input pull-up
- JTDI: Input pull-up
- JTMS/SWDIO: Input pull-up
- JTCK/SWCLK: Input pull-down
- JTDO: Input floating

The software can then use these I/Os as standard GPIOs.

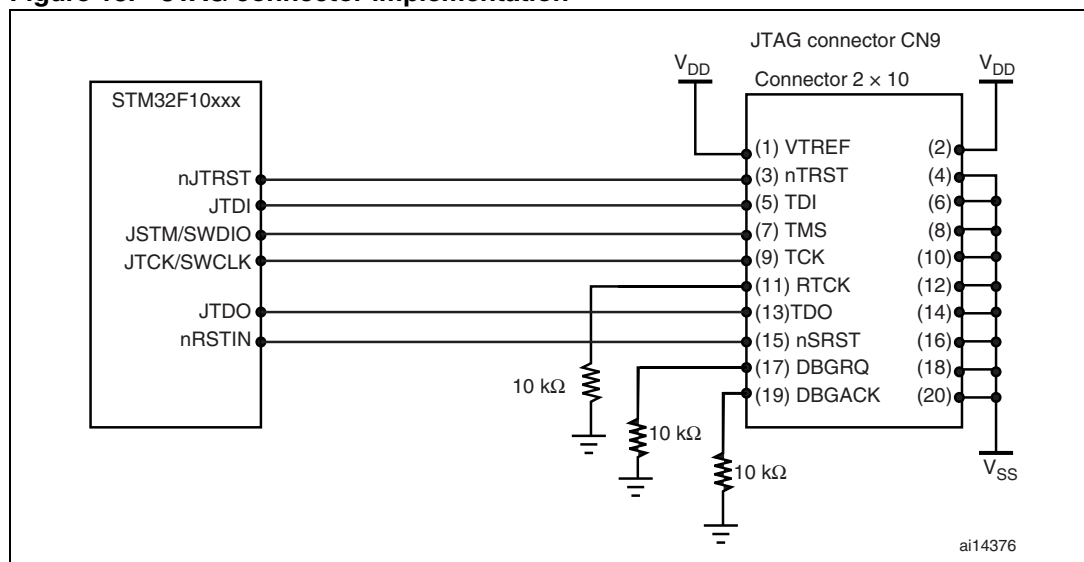
*Note: The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but there is no special recommendation for TCK. However, for the STM32F10xxx, an integrated pull-down resistor is used for JTCK.*

*Having embedded pull-up and pull-down resistors removes the need to add external resistors.*

### 4.3.4 SWJ debug port connection with standard JTAG connector

Figure 13 shows the connection between the STM32F10xxx and a standard JTAG connector.

**Figure 13. JTAG connector implementation**



## 5 Recommendations

### 5.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground ( $V_{SS}$ ) and another dedicated to the  $V_{DD}$  supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

### 5.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

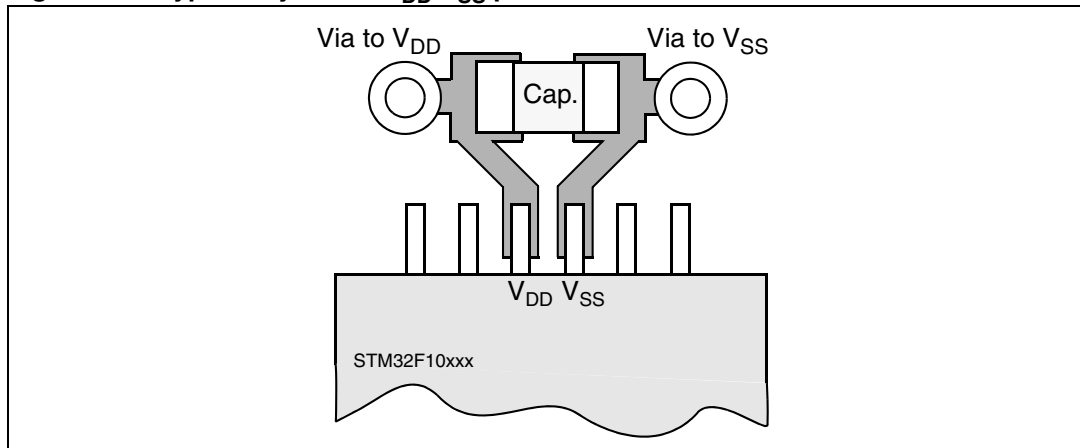
### 5.3 Ground and power supply ( $V_{SS}$ , $V_{DD}$ )

Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. The power supply should be implemented close to the ground line to minimize the area of the supply loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

### 5.4 Decoupling

All pins need to be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors  $C$  (100 nF) and a chemical capacitor  $C$  of about 10  $\mu$ F connected in parallel on the STM32F10xxx device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. [Figure 14](#) shows the typical layout of such a  $V_{DD}/V_{SS}$  pair.

**Figure 14. Typical layout for  $V_{DD}/V_{SS}$  pair**

## 5.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- signals for which a temporary disturbance affects the running process permanently (the case of interrupts and handshaking strobe signals, and not the case for LED commands).  
For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.  
For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- noisy signals (clock, etc.)
- sensitive signals (high impedance, etc.)

## 5.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, unused clocks, counters or I/Os, should not be left free, e.g. I/Os should be set to “0” or “1”(pull-up or pull-down to the unused I/O pins.) and unused features should be “frozen” or disabled.

## 6 Reference design

### 6.1 Description

The reference design shown in [Figure 15](#), is based on the STM32F103ZE(T6), a highly integrated microcontroller running at 72 MHz, that combines the new Cortex™-M3 32-bit RISC CPU core with 512 Kbytes of embedded Flash memory and up to 64 Kbytes of high-speed SRAM.

This reference design can be tailored to any other STM32F10xxx device with different package, using the pins correspondence given in [Table 6: Reference connection for all packages](#).

#### 6.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X1– 32.768 kHz crystal for the embedded RTC
- HSE: X2– 8 MHz crystal for the STM32F10xxx microcontroller

Refer to [Section 2: Clocks on page 11](#).

#### 6.1.2 Reset

The reset signal in [Figure 15](#) is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to [Section 1.3: Reset & power supply supervisor on page 8](#).

#### 6.1.3 Boot mode

The boot option is configured by setting switches SW2 (Boot 0) and SW1 (Boot 1). Refer to [Section 3: Boot configuration on page 16](#).

*Note:* In low-power mode (more specially in Standby mode) the boot mode is mandatory to be able to connect to tools (the device should boot from the SRAM).

#### 6.1.4 SWJ interface

The reference design shows the connection between the STM32F10xxx and a standard JTAG connector. Refer to [Section 4: Debug management on page 18](#).

*Note:* It is recommended to connect the reset pins so as to be able to reset the application from the tools.

#### 6.1.5 Power supply

Refer to [Section 1: Power supplies on page 6](#).

## 6.2 Component references

**Table 4. Mandatory components**

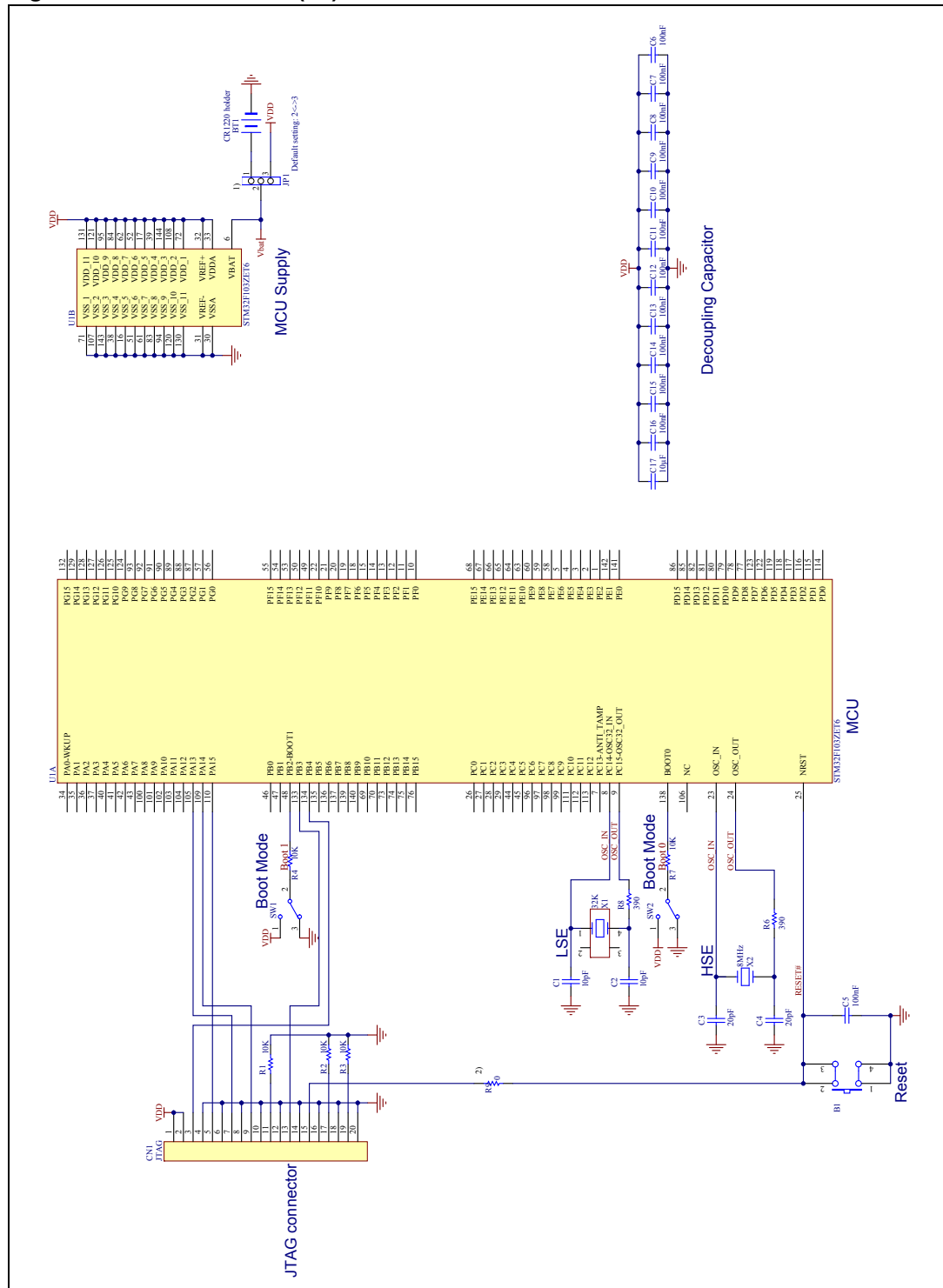
Id	Components name	Reference	Quantity	Comments
1	Microcontroller	STM32F103ZE(T6)	1	144-pin package
2	Capacitors	100 nF	11	Ceramic capacitors (decoupling capacitors)
3	Capacitor	10 $\mu$ F	1	Ceramic capacitor (decoupling capacitor)

**Table 5. Optional components**

Id	Components name	Reference	Quantity	Comments
1	Resistor	10 k $\Omega$	5	pull-up and pull-down for JTAG and Boot mode.
2	Resistor	390 $\Omega$	1	used for HSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example.
3	Resistor	0 $\Omega$	1	used for LSE: the value depends on the crystal characteristics. This resistor value is given only as a typical example.
4	Capacitor	100 nF	1	Ceramic capacitor
5	Capacitor	10 pF	2	used for LSE: the value depends on the crystal characteristics.
6	Capacitor	20 pF	2	used for HSE: the value depends on the crystal characteristics.
7	Quartz	8 MHz	1	used for HSE
8	Quartz	32 kHz	1	used for LSE
9	JTAG connector	HE10	1	
10	Battery	3V3	1	If no external battery is used in the application, $V_{BAT}$ must be connected externally to $V_{DD}$
11	Switch	3V3	2	Used to select the right boot mode
12	Push-button	B1	1	



Figure 15. STM32F103ZE(T6) microcontroller reference schematic



1. If no external battery is used in the application,  $V_{BAT}$  must be connected externally to  $V_{DD}$
2. To be able to reset the device from the tools this resistor has to be kept.

Table 6. Reference connection for all packages

Pin name	Pin numbers for LQFP packages				Pin numbers for BGA packages		Pin numbers for VFQFPN package
	144 pins	100 pins	64 pins	48 pins	144 pins	100 pins	36 pins
OSC_IN	23	12	5	5	D1	C1	2
OSC_OUT	24	13	6	6	E1	D1	3
PC15-OSC32_OUT	9	9	4	4	C1	B1	-
PC14-OSC32_IN	8	8	3	3	B1	A1	-
BOOT0	138	94	60	44	D5	D5	35
PB2-BOOT1	48	37	28	20	J5	G5	17
NRST	25	14	7	7	F1	E1	4
PA13	105	72	46	34	A12	A10	25
PA14	109	76	48	37	A11	A9	28
PA15	110	77	50	38	A10	A8	29
PB4	134	90	56	40	A6	A6	31
PB3	133	89	55	39	A7	A7	30
V <sub>SS_1</sub>	71	49	31	23	H7	E7	18
V <sub>SS_2</sub>	107	74	47	35	G9	E6	26
V <sub>SS_3</sub>	143	99	63	47	E5	E5	36
V <sub>SS_4</sub>	38	27	18	-	G4	E4	-
V <sub>SS_5</sub>	16	10	-	-	D2	C2	-
V <sub>SS_6</sub>	51	-	-	-	H5	-	-
V <sub>SS_7</sub>	61	-	-	-	H6	-	-
V <sub>SS_8</sub>	83	-	-	-	G8	-	-
V <sub>SS_9</sub>	94	-	-	-	G10	-	-
V <sub>SS_10</sub>	120	-	-	-	E7	-	-
V <sub>SS_11</sub>	130	-	-	-	E6		-
V <sub>DD_1</sub>	72	50	32	24	G7	F7	19
V <sub>DD_2</sub>	108	75	48	36	F9		27
V <sub>DD_3</sub>	144	100	64	48	F5	F5	1
V <sub>DD_4</sub>	39	28	19	-	F4	F4	-
V <sub>DD_5</sub>	17	11	-	-	D3	D2	-
V <sub>DD_6</sub>	52	-	-	-	G5	-	-
V <sub>DD_7</sub>	62	-	-	-	G6	-	-
V <sub>DD_8</sub>	84	-	-	-	F8	-	-

Table 6. Reference connection for all packages (continued)

Pin name	Pin numbers for LQFP packages				Pin numbers for BGA packages		Pin numbers for VFQFPN package
	144 pins	100 pins	64 pins	48 pins	144 pins	100 pins	36 pins
V <sub>DD_9</sub>	95	-	-	-	F10	-	-
V <sub>DD_10</sub>	121	-	-	-	F7	-	-
V <sub>DD_11</sub>	131	-	-	-	F6	-	-
V <sub>REF+</sub>	32	21	-	-	L1	J1	-
V <sub>REF-</sub>	31	20	-	-	K1	H1	-
V <sub>SSA</sub>	30	19	12	8	J1	G1	-
V <sub>DDA</sub>	33	22	13	9	M1	K1	-
V <sub>BAT</sub>	6	6	1	1	C2	B2	-

## 7 Revision history

**Table 7. Document revision history**

Date	Revision	Changes
12-Jul-2007	1	Initial release.
23-May-2008	2	Application note also applicable to High-density devices. <i>Figure 1: Power supply overview</i> , <i>Figure 2: Power supply scheme</i> and <i>Figure 6: Clock overview</i> updated. Low-speed internal RC frequency modified in <i>Section 2: Clocks on page 11</i> . $V_{REF+}$ voltage range modified. <i>Table 6: Reference connection for all packages on page 26</i> added. Small text changes.

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